1. Minimal SOP: \( F = ab'c' + abd + ab'd' \) or \( F = abd + a'b'd' + ac'd \)

   Minimal POS: \( F = a(b' + d)(b + c' + d') \)

2. a) \( z_1 = a'b'd' + b'c'd \)

   b) \( z_2 = a'bd' + bcd \)

   c) \( z_3 = ab + a'b'c \)
3. Circuit diagram

- Note that this is a set input, not a reset.
- The other FF's have reset tied to a reset input.
There are many correct answers to this problem, depending upon which variables are connected to the select lines and what order they are in.
5. 

(a) 2’s complement

\[
\begin{array}{c}
011010 \\
+ 110011 \\
\hline
1001101 \quad (13)
\end{array}
\]

Ignore carry in to last bit = carry out, so no overflow.

1’s complement

\[
\begin{array}{c}
011010 \\
110010 \\
\hline
\hline
001100 \quad (13)
\end{array}
\]

\[\text{carryout wraps around in 1’s complement subtraction}\]

(b) 2’s complement

\[
\begin{array}{c}
010010 \\
101101 \\
\hline
111111 \quad (-1)
\end{array}
\]

1’s complement

\[
\begin{array}{c}
010010 \\
101100 \\
\hline
111110 \quad (-1)
\end{array}
\]