Supplemental Slides:

MIMO Testbed Development at the MPRG Lab

Raqibul Mostafa
Jeffrey H. Reed
Overview

- **Space Time Coding (STC) Overview**
- **Virginia Tech Space Time Adaptive Radio (VT-STAR) description:**
  - System Architecture, RF Specs, TX/RX system,
  - Interface, DSP Implementation, Indoor channel measurements
- **SDR-3000**
Space Time Coding (STC) Overview
\[(n_T, n_R) - \text{ ( \# of Tx. Ant., \# of Rx. Ant.)}\]

\[
r_t^j = \sum_{i=1}^{n_T} \alpha_{ij} \cdot c_t^i + \eta_t^j + \text{ISI} + \text{MAI} \quad j = \{1, 2, \ldots, n_R\}
\]
Background

- Space-time codes were proposed by Tarokh et. al. in the 1997 International Symposium on Information Theory (ISIT).
- Capacity analysis of the MIMO channel was proposed by Foschini and Gans of Lucent Technologies in 1997.

Features of STC

- Move diversity burden from mobile to base station
- Diversity advantage
- Coding gain
- Increased bandwidth efficiency
STBC Operation

Space-Time Block Encoding

\[ h_{22} = \alpha_{22} e^{j\theta_{22}} \]
\[ h_{12} = \alpha_{12} e^{j\theta_{12}} \]
\[ h_{21} = \alpha_{21} e^{j\theta_{21}} \]
\[ h_{11} = \alpha_{11} e^{j\theta_{11}} \]

Channel Estimation

\[ \hat{h}_{12} \]
\[ \hat{h}_{22} \]
\[ \hat{h}_{11} \]
\[ \hat{h}_{21} \]

Combiner

\[ \hat{s}_0 \]
\[ \hat{s}_1 \]

Maximum Likelihood Detector

\[ i = \min_k \left[ d^2 (\hat{s}_0, s_k) \right] \]

Transmit Antenna 1

<table>
<thead>
<tr>
<th>Time t</th>
<th>Transmit Antenna 1</th>
<th>Transmit Antenna 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>S_0</td>
<td></td>
<td>S_1</td>
</tr>
<tr>
<td>-S*_{-1}</td>
<td></td>
<td>S*_{0}</td>
</tr>
</tbody>
</table>

Time

Space

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- mutually uncorrelated Rayleigh fading channels
- Channel flat for one block of STBC
- perfect knowledge of channel state information (CSI) at the receiver
- Total Tx power same
- Rx Signal power for MRRC 3 dB more than C-STBC
VT-STAR: A 2×2 MIMO Testbed
Introduction

- **Objective:**
  - To build a testbed to demonstrate the utility of MIMO techniques and to provide with MIMO indoor channel measurements
  - Testbed development based on software defined radio (SDR) approach for flexibility and reconfigurability
  - DSP processing platform for both the transmitter and the receiver
  - Implemented MIMO technique based on Space Time Block Code (STBC)
  - Other MIMO techniques also possible through DSP programming
VT-STAR System Architecture

- RF Section
- Data Conversion
- DSP Core
- Application Layer (Host)
### RF Specifications

<table>
<thead>
<tr>
<th>RF Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Center Frequency</td>
<td>2050 MHz</td>
</tr>
<tr>
<td>Maximum Signal Bandwidth</td>
<td>750 kHz</td>
</tr>
<tr>
<td>Receiver Noise Floor</td>
<td>-110 dBm</td>
</tr>
<tr>
<td>Maximum Receiver Input Power</td>
<td>-50 dBm</td>
</tr>
<tr>
<td>Spurious-Free Dynamic Range (SFDR)</td>
<td>60 dB</td>
</tr>
<tr>
<td>Transmitter Input</td>
<td>Baseband I/Q, 35 mV RMS</td>
</tr>
<tr>
<td>Receiver Output</td>
<td>Baseband I/Q, 140 mV RMS</td>
</tr>
<tr>
<td>Transmit Power (Maximum/Nominal)</td>
<td>26dBm / 0 dBm</td>
</tr>
<tr>
<td>Transmitter/Receiver Input/Output Impedance</td>
<td>50Ω</td>
</tr>
</tbody>
</table>
Multi-Channel RF Receiver

- **BPF**
  - fc 2050 MHz
  - BW < 100 MHz

- **ZEM4300**
  - ZFL-1000GH

- **AGC Integrator**
  - fc 68 MHz
  - BW3dB > 1.2 MHz
  - BW50dB < 1.5 MHz

- **I/Q Demod**
  - ZFMIQ-70D
  - To TITM THS 1206 boards
  - BWmax=600 kHz

- **BPF**
  - fc 68 MHz
  - BW3dB > 1.2 MHz
  - BW50dB < 1.5 MHz

- **Splitter ZESC-2-11**

- **From TITM TMS320C67 EVM**
Synchronization of 4 DAC EVMs

- DAC4
  - Q2
  - D11-D4
  - CLK

- DAC3
  - I2
  - D11-D4
  - CLK

- DAC2
  - Q1
  - D11-D4
  - CLK

- DAC1
  - I1
  - CLK
  - D11-D4

- XD31-XD24
- XD23-XD16
- XD15-XD8
- XD7-XD0

- XD1-D4
- XD3-XD0

- XWE

- DSK J1 interface
C6701 DSP

- 32 bit Floating point DSP
- Advanced VelociTI VLIW architecture
- 133 MHz
- 1064 MFLOPs
- 2 MACs per cycle
- 32 general-purpose registers
- Eight highly independent functional units
- Integrated Development Environment (IDE)
  Code Composer
Transmitter: DSP Implementation

Flowchart

Source (PN Generator)

QPSK Mapping

M Mapping

Differential Encoding

Space-Time Block Coding

Delay

Pulse Shaping I1

Pulse Shaping Q1

Pulse Shaping I2

Pulse Shaping Q2

Data Packing

To 4xT1™ THS1556 EVMs

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DSP Host Communication

- **Real-time data exchange (RTDX)**
  - bi-directional real-time transfer between DSP and the host PC

- **Application Layer of radio**
  - Display key parameters of physical layer in MATLAB
  - Collect data for offline post-processing
  - Modify a video sequence on a video Emulator
• The TX and RX subsystems were connected back-to-back: The DACs and the ADCs were directly connected
• Channel estimates showed that direct components ($h_{11}$ and $h_{22}$) were much stronger than the cross components ($h_{21}$ and $h_{12}$): about 25 dB higher
• This setup validates the system.
Measurement set up

- Lab with desks, workbenches, and metallic shelves
- Line Of Sight & Non line of sight (NLOS) considered
- Transmitter and receiver placed in fixed locations before measurement
Measured Channel capacity

A key result for flat Rayleigh fading channels (Foschini and Gans) 
\((n_T, n_R)\): ( # of Tx. Ant., # of Rx. Ant.)

\(H\): Channel matrix of fade coefficients

\[ C = \log_2 \det \left[ I_n + \left( \frac{SNR}{n_T} \right) H \cdot H^\dagger \right] \]

Channel Capacity over time

Histogram

VT-STAR Channel Capacity per path; \(n_T = 2; n_R = 2\); Non-Line-of-Sight Measurements

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Introduction

- **SDR-3000** is a versatile wideband multi-channel transceiver testbed:
  - Real-time implementation of communications systems
  - Baseband algorithm development and verification
  - Wideband MIMO algorithm demonstration
  - MIMO channel measurement and characterization

- **SDR-3000** offers communications system design and implementation using *software defined radio* (SDR) concepts
**SDR-3000 Basic Features**

- Combines Xilinx Vertix FPGA with MPC7410 G4s in a single system
- Supports 4 ADC at 80MHz
- Supports 4 DACs at 80/160MHz
- Support high density and/or high performance software defined radios
- SDR can support 10s of separate transmit and receive channels, each with independent air interface protocol.
- Multiple air interface supported by software
- Software Communications Architecture (SCA) compliant multi-channel software radio transceiver system
SCA Overview

- Now a joint project of JTRS and SDR Forum – most participants are members of both

- An attempt to develop a “universal” SDR architecture (five identified domains)
  - Emerging standard for software radio compliance

- Still a work in progress - Currently v2.2

- SCA - Important step to enable widespread use of software radios
  - Develops an object oriented approach to radio design
  - Enables independent vendors to develop software modules that are compatible with each other
System Description

- 3 cPCI-based boards
  - TM1-3300: Analog I/O board supporting 2 80MHz ADCs and DACs
  - PRO-3100: High speed processing board with 4 user programmable Xilinx Virtex-II FPGAs, and 1 MPC7410 PowerPC
  - Pro-3500: Signal processing board with 2 G4 PowerPCs and 1 MPC7410 PowerPC for controlling the board
SDR-3000 Transceiver Subsystem

Stage 1: RF
Stage 2: Analog Interface
Stage 3: Digital Interface
Stage 4: Baseband Data, Encoded
Stage 5: Single Board Computer

Air Interface
High Frequency
Analog Intermediate Frequency
Digital Intermediate Frequency
Baseband Data, Encoded
Baseband Data, Decoded

From Spectrum Signal Processing

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SDR-3000 Testbed Goals

- Build a testbed based on SDR 3000 for MIMO testing
- Perform IF digital up and down conversion operations within the PRO-3500.
- Signaling format: OFDM based physical layer.
- TX RF front-end: VTSTAR transmitter
- RX RF front-end: SIGNIA 9136 receiver
IF sampling frequency: 65 MHz (4 times over sampled)
Bandwidth used: 17.56 MHz
Current status

- Implemented 802.11a based OFDM physical layer baseband on PRO-3500
- Validated on SDR-3000 using TX/RX loop back
- Digital up and down conversion from base band to IF tested on SDR-3000 through loop back.
- RF front end tested through loop back.
- IF to RF integration in progress.