Bias-T Design Considerations for the LWA

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The strawman design document [1] for the LWA suggests that the Front End Electronics (FEE) could be powered through the use of a circuit known as a bias-T. We will discuss how a bias-T operates and present a low cost design optimized for performance within the LWA frequency range of 20 to 80 MHz. We highly recommend the use of bias-T based on discrete components incorporated directly into the LWA FEE and ARX subsystems.

I. Introduction

A bias-T is a three port network designed to provide power to remote devices, such as amplifiers, over the same coaxial cable that RF signals are conveyed. The basic topology, and means of operation, of a bias-T network suitable for LWA applications is given in Figure 1.

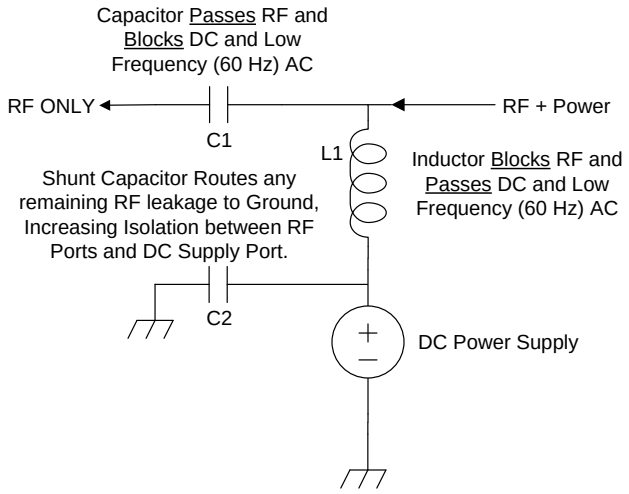


Figure 1 – Basic 'Inductive' Bias-T

Commercially available bias-Ts are available in both "connectorized" and surface mount versions. These units are typically expensive ($40 to $100) and, although designed to be wideband, often suffer in performance at frequencies below 50 MHz.

By concentrating on an LWA specific bias-T we can achieve a significant cost savings. We will focus on presenting a bias-T circuit that is optimized for operation below 100 MHz and has the ability to supply a single polarization of an LWA FEE (230 mA). We will also deliver a circuit with a compact printed circuit board (PCB) footprint.

II. LWA Bias-T Design Considerations

Consisting of one inductor and one capacitor the bias-T circuit is simple, but particular consideration must be given to component selection. Although not a part of the generic bias-T circuit, the shunt capacitor (C2) on the DC port should not be considered optional (Figure 1). Addition of this capacitance substantially increases isolation between the RF ports and the DC supply connection by routing any remaining RF leakage on the supply side of the inductor to ground (Figures 11, 12, and 13).

It is especially important that the inductor be rated for the necessary current and should optimally have a minimum self resonant frequency (SRF) that is above the highest LWA frequencies. Throughout the entire LWA band, the inductor must present high impedance, and both capacitors must present low impedance; resonances must be avoided.

Based on research and experience, we have selected the following components for consideration and testing:

Capacitors (C1, C2):	0.1 μF Ceramic Capacitor (SMT 1208), Panasonic, ECJ-3VB1E104K
Inductor (L1):	4.7 μH Wirewound Inductor (SMT 1008), Delevan, 1008-472J

III. LWA Bias-T Prototyping

We have produced a PCB layout to enable us to reliably evaluate the performance of our bias-T with a variety of components (Figure 2). The SMA connectors featured here are only included as a convenience for testing. The basic orthogonal arrangement of L1 and C1 can be readily incorporated into the FEE and ARX regardless of the connectors these subsystems utilize.

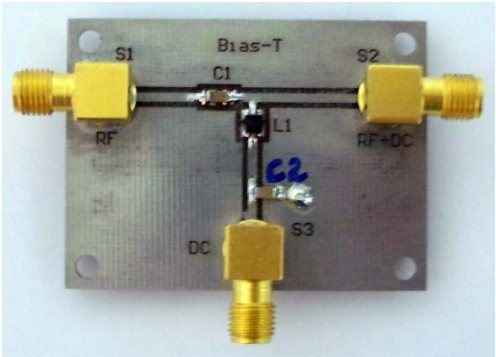


Figure 2 – Bias-T Evaluation Board

The circuit was evaluated both as a single unit and in the intended configuration with two bias-Ts connected together and transferring power. In the configurations with two bias-Ts, we supplied 15 VDC at ~240 mA to a power-resistor load (~3.6 Watts dissipated) throughout the test (Figure 3). It was our intention to evaluate the performance of the inductors in the circuit while operating under load conditions representative of a G250R balun (FEE).

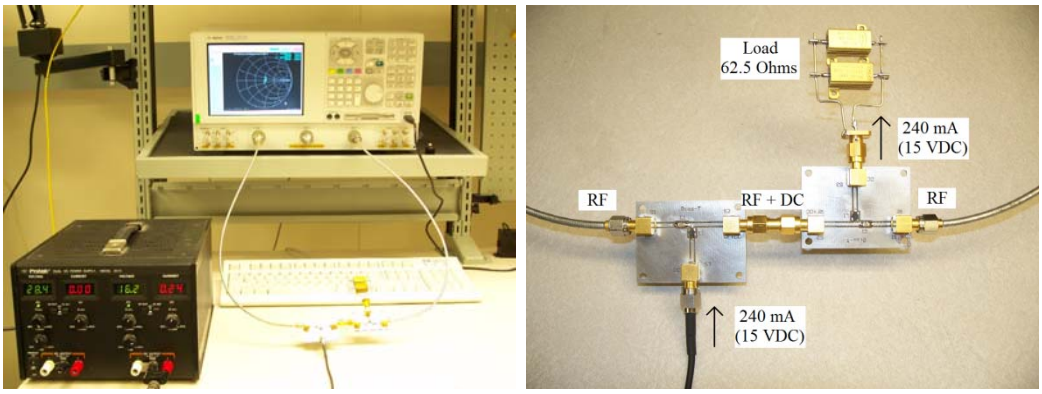


Figure 3 – Characterization of the Bias-T Operating under Load

In the single unit configurations we placed an SMA "short" on the DC port of the bias-T. It was our intention here to capture the performance of the single bias-T when connected to a DC power supply with very low output impedance.

An Agilent N3383A vector network analyzer was used to characterize insertion loss (S21), return loss (S11 and S22), and isolation (S21 between RF and DC ports). A complete set of data is included in the measurements section of this report.

IV. Observations and Recommendations

The performance of the bias-T presented here is comparable to designs that we have already fielded and found to be entirely successful in operation. Within the LWA band, the performance of this circuit compares favorably to costly commercial units. The insertion loss of *two* of these cascaded bias-Ts was found to be less than 0.2 dB, and the aggregate return loss was found to be least -20 dB.

RF coupling from one dipole to another through the DC power network is a serious concern and potential source of indirect mutual coupling. It is important that significant attenuation be presented between the RF ports and the DC supply node of the bias-T. Direct mutual coupling between elements at a spacing of 4m has been demonstrated to be approximately -20 dB, declining ~5 dB for each 2m increase in spacing [2]. After 20 meters the mutual coupling between elements is approximately -60 dB and only gradually diminishes with additional spacing [2]. Consequently, we recommend that feed system coupling be kept well below -80 dB.

The most expedient means of accomplishing this goal is the introduction of a capacitive shunt on the DC side of the bias-T. This can be seen on the schematic (Figure 14) as capacitor C2. It is typically a part of good engineering practice to incorporate "bypass capacitors" (such as C2) at DC supply nodes; we provide measurements here to emphasize the consequences of omitting this component. The isolation between the RF port and DC port of the bias-T *without* the capacitive shunt is seen to be inadequate in Figure 11. A definite improvement in isolation is seen when a 0.1 μF shunt is added at

the DC supply node (Figure 12). With the shunt, at least 60 dB of attenuation between the RF ports and the DC supply port is achieved. An RF signal must run the gauntlet of two of networks consisting of L1 and C2 to traverse the DC feed ports of two bias-Ts and get from one dipole signal chain to another. Greater than 100 dB of attenuation is observed in this configuration (Figure 13).

The prototype circuit fits within an 8.3 x 10 mm square on the circuit board; PCB space constraints should not be problematic.

We recommend the use of a high-capacity DC power supply to supply power to the FEEs via a bias-T arrangement such as discussed here. This method of power distribution will spare the cost of installing and maintaining a separate power distribution network and eliminate unnecessary complexity in station installations. Because DC power is sourced via the center conductor of shielded coaxial cable, the resulting power network is effectively shielded at no additional cost. Candidate connectors for LWA RF cabling will likely incorporate conductive backshells which will act to further inhibit the introduction of RFI via the power distribution network.

By incorporating a bias-T into the ARX, the option of allowing power to the antenna stands to be under control of the LWA Monitor and Control System (MCS) becomes inexpensive and straightforward to implement. This feature could prove valuable for diagnostics, maintenance, and station commissioning.

V. Summary Table

Operating Frequency	15 to 115 MHz
Isolation	60 dB Minimum
Insertion Loss	0.2 dB Maximum
VSWR	1.2:1 Maximum
Maximum DC Voltage	25 VDC
Maximum DC Current	334 mA
Size	PCB Footprint Approximately 8.3 x 10 mm
Parts Cost	$0.92

VI. Measurements: *-30 dBm Power Level for RF Stimulus*

1. Measurements of a Single Bias-T

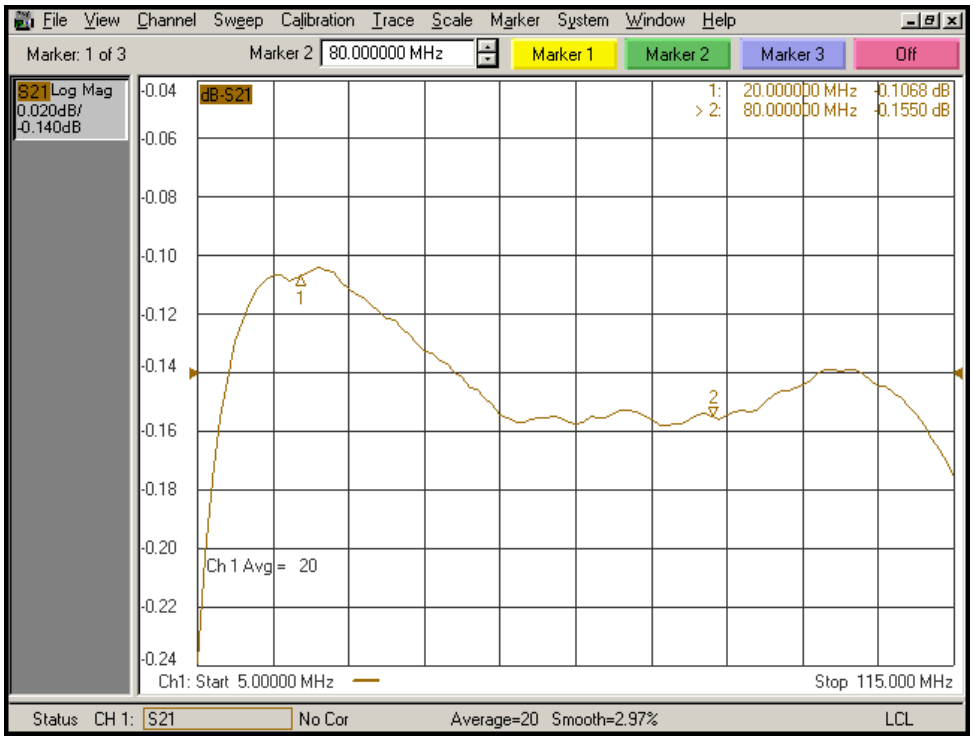


Figure 4 – Insertion Loss (S21) through a Single Bias-T with DC Port Shorted

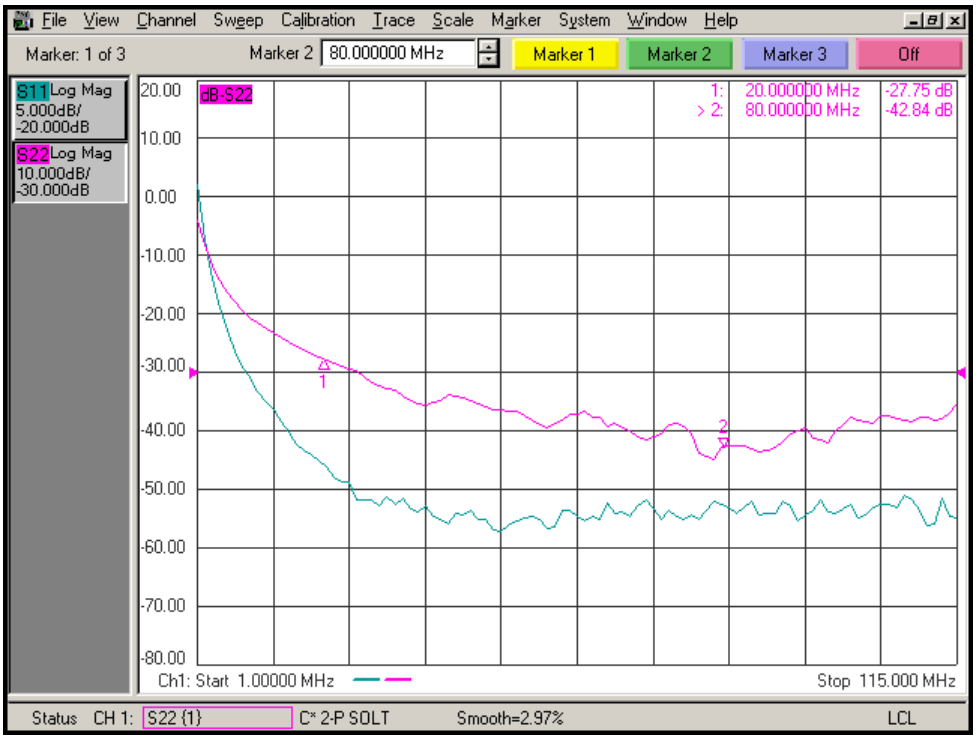


Figure 5 – Return Loss (S11 and S22) into a Single Bias-T with DC Port Shorted

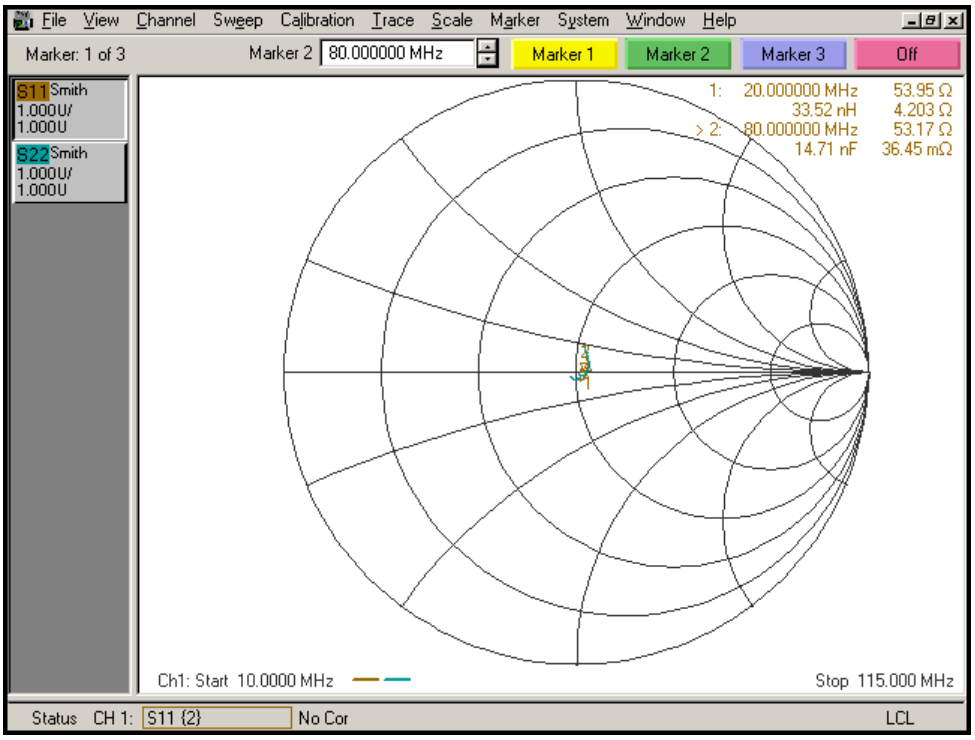


Figure 6 – Return Loss (S11 and S22) into a Single Bias-T with DC Port Shorted (Smith)

2. Measurements of a Two Bias-Ts in Cascade Delivering 240 mA to a Load

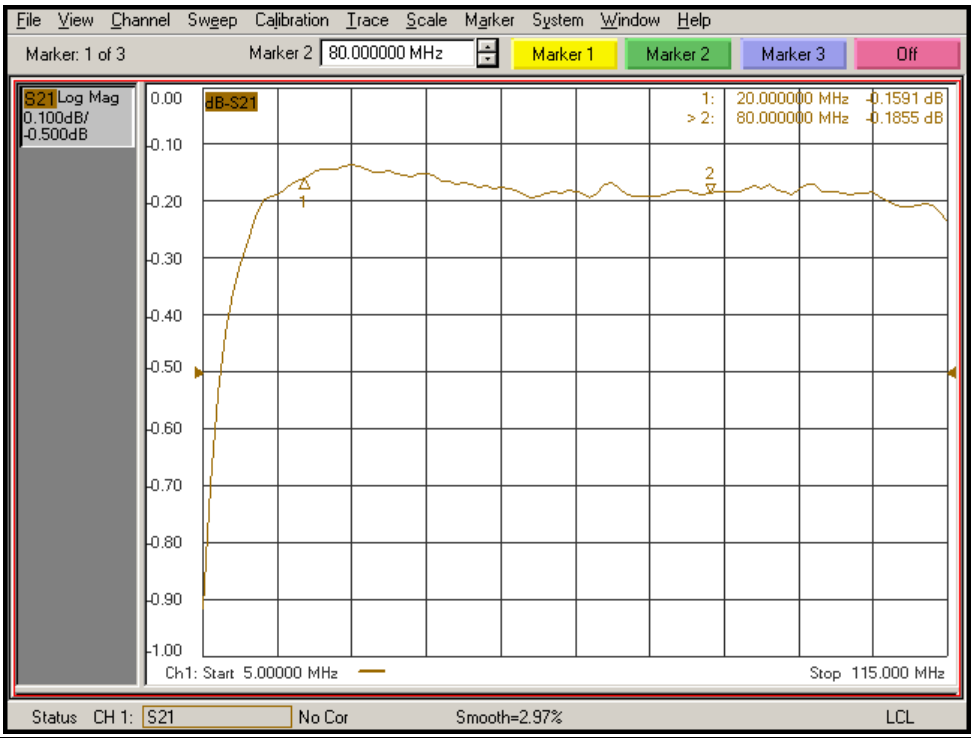


Figure 7 – Insertion Loss through Two Bias-T Supplying 240 mA to a Resistive Load

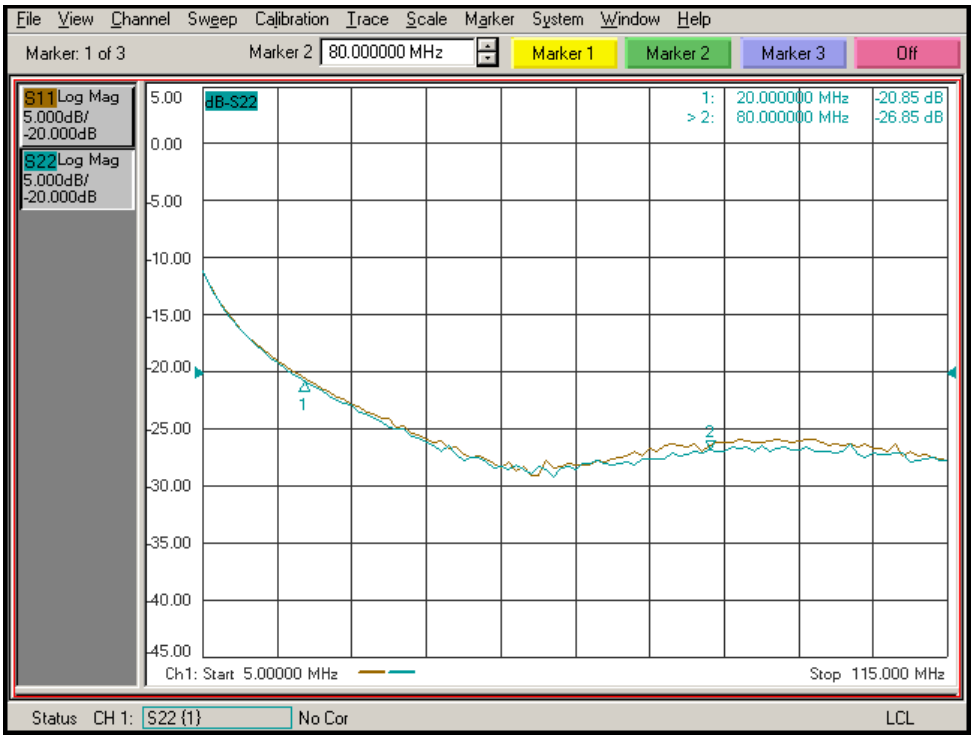


Figure 8 – Return Loss (S11 and S22) into Two Cascaded Bias-Ts Delivering 240 mA

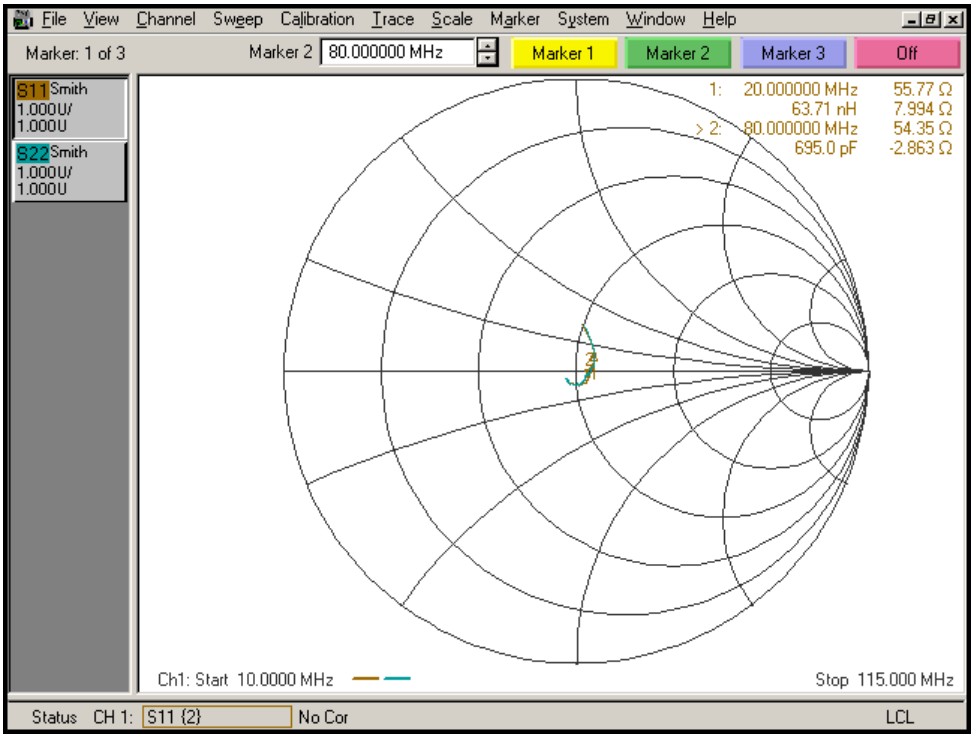


Figure 9 – Return Loss (S11 and S22) into Two Cascaded Bias-Ts Delivering 240 mA (Smith)

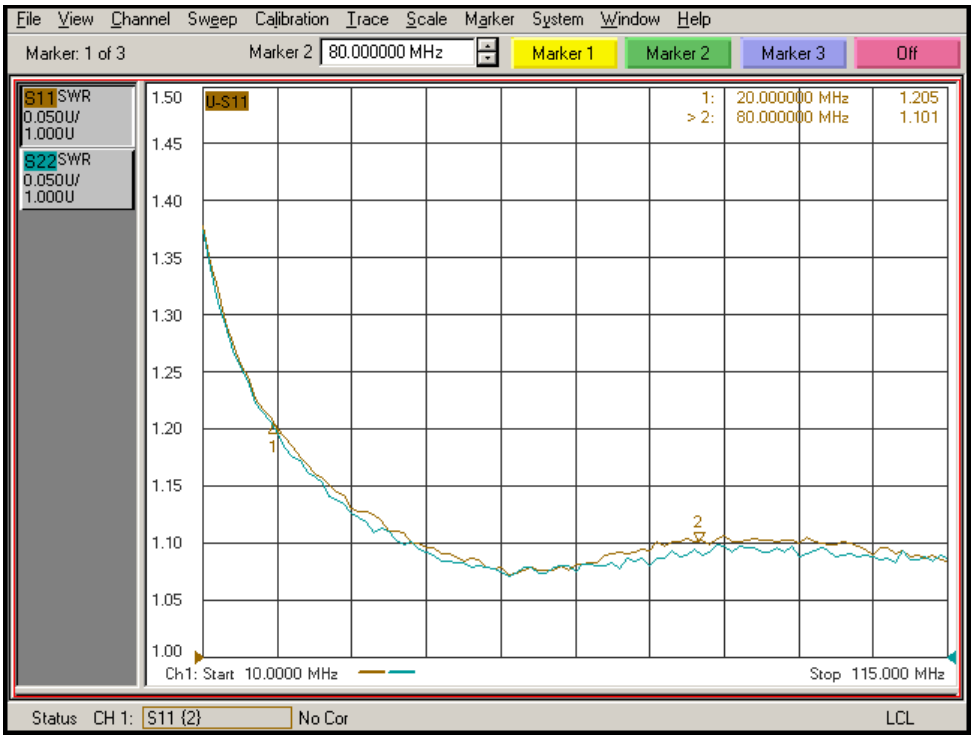


Figure 10 – SWR (S11 and S22) into Two Cascaded Bias-Ts Delivering 240 mA

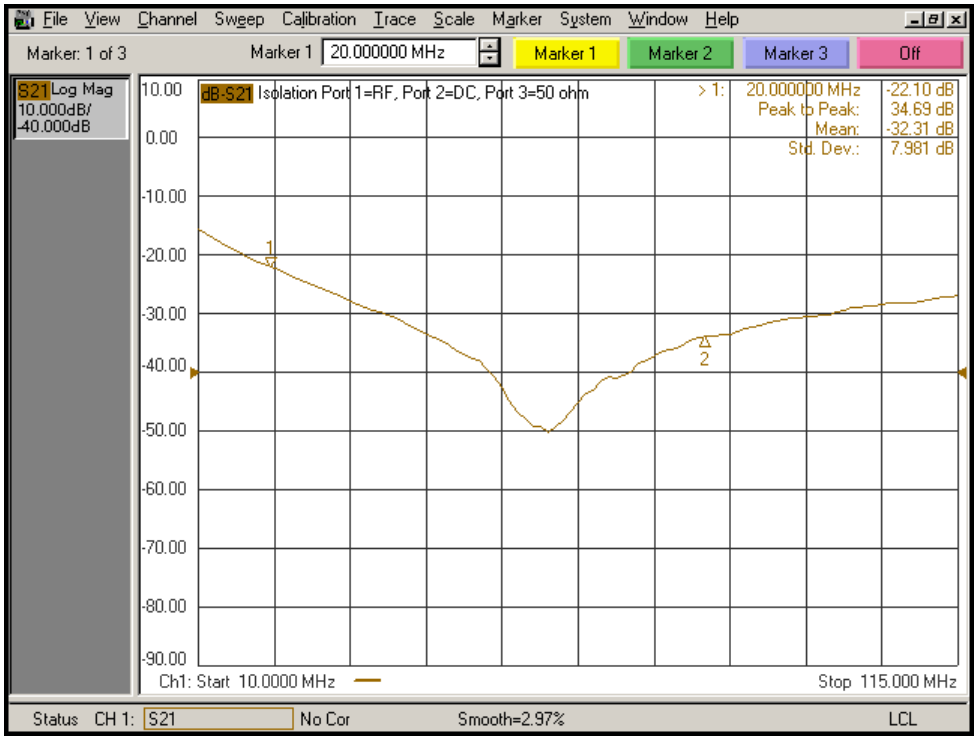


Figure 11 – Single Bias-T Isolation between RF and DC Port *without* Capacitive Shunt. RF+DC Port 50Ω Terminated

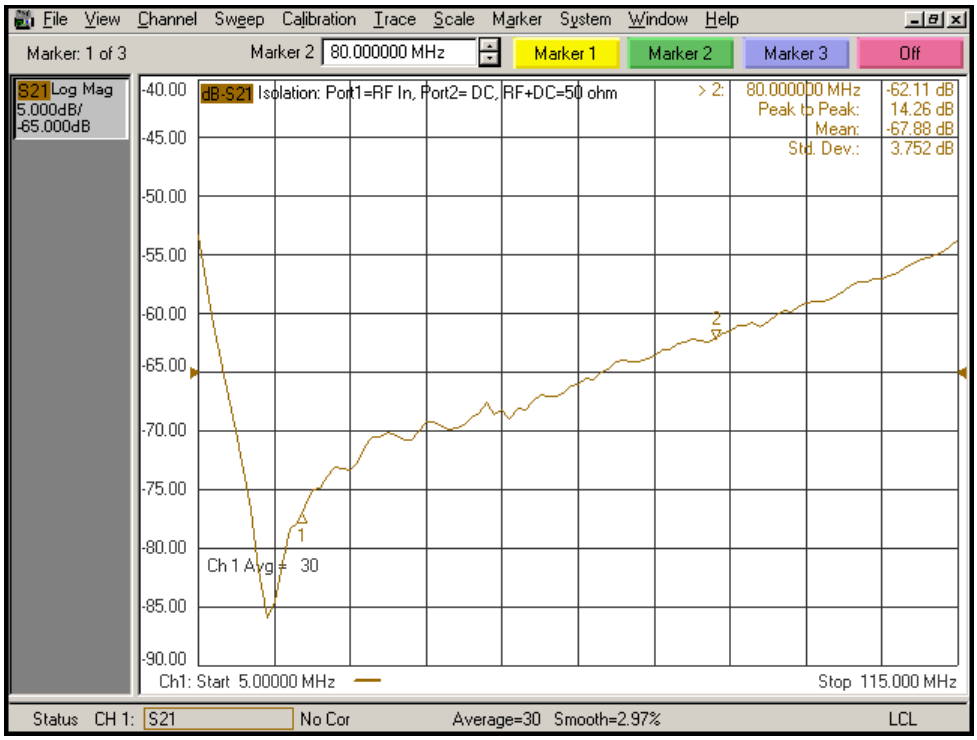


Figure 12 – Single Bias-T - Isolation between RF and DC Port *with* Capacitive Shunt (0.1 µF).
RF+DC Port 50Ω Terminated

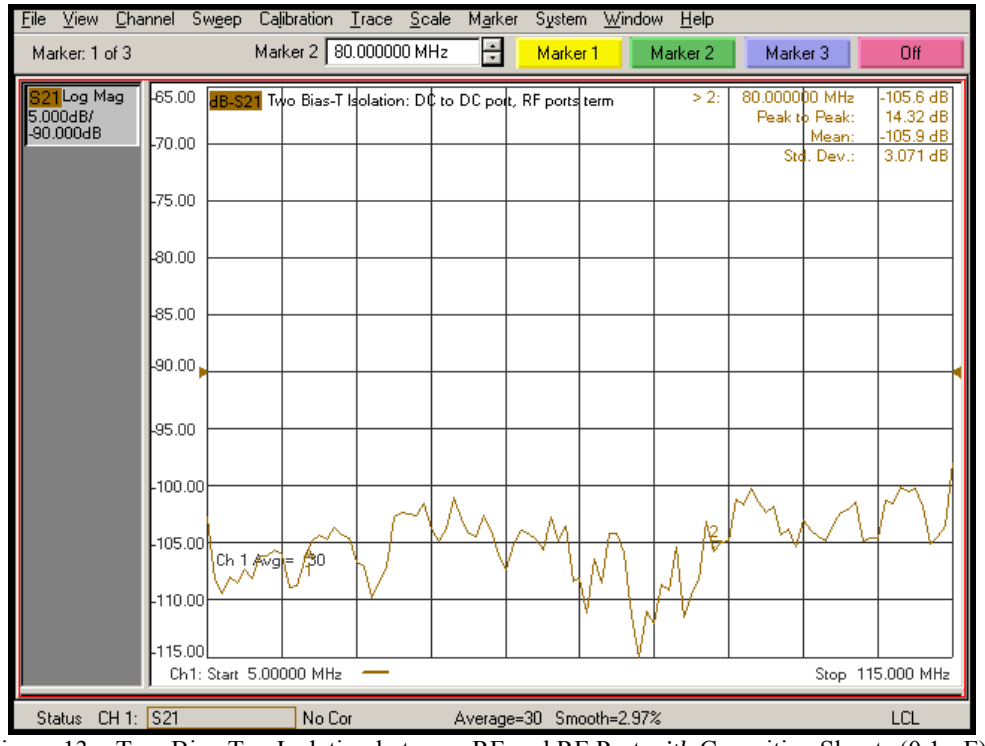


Figure 13 – Two Bias-Ts - Isolation between RF and RF Port *with* Capacitive Shunts (0.1 µF).
RF ports 50Ω Terminated.
Note: A power level of *0 dBm* was used for this measurement.

VII. Bill of Materials

Designation	Value	Tolerance	Type	Manufacturer Part No.	Cost
C1, C2	0.1 μF	10%	Capacitor, Ceramic	Panasonic ECJ-3VB1E104K	$0.056 (Quantities > 4000)
L1	4.7 μH	+/- 5%	Inductor, Unshielded (1206), X7R	Delevan 1008-472J	$0.81 (Quantities > 2000)

Total cost for each bias-T: $0.92
Total cost each antenna stand (4 bias-Ts, two per polarization): $3.69

The results presented here are based on the use of Delevan part '1008-472J' for L1. Alternatively, part 'WW1008-472R' could also be used. The former part is less expensive, and more readily available. Specifications for both parts are provided in the datasheet section at the end of this report.

VIII. References

[1] "A Strawman Design for the Long Wavelength Array Stations", P.S. Ray (et. Al), April 11, 2006, http://www.ece.vt.edu/swe/lwa/memo/lwa0035.pdf, LWA Memo #35.

[2] "Report on Mutual Coupling and Impedance Measurements on Large Blade Dipoles", B. Erickson, H. Schmitt, E. Polisensky, August 28, 2006, http://www.ece.vt.edu/swe/lwa/memo/lwa0053.pdf, LWA Memo #53.

IX. Schematics and Layouts

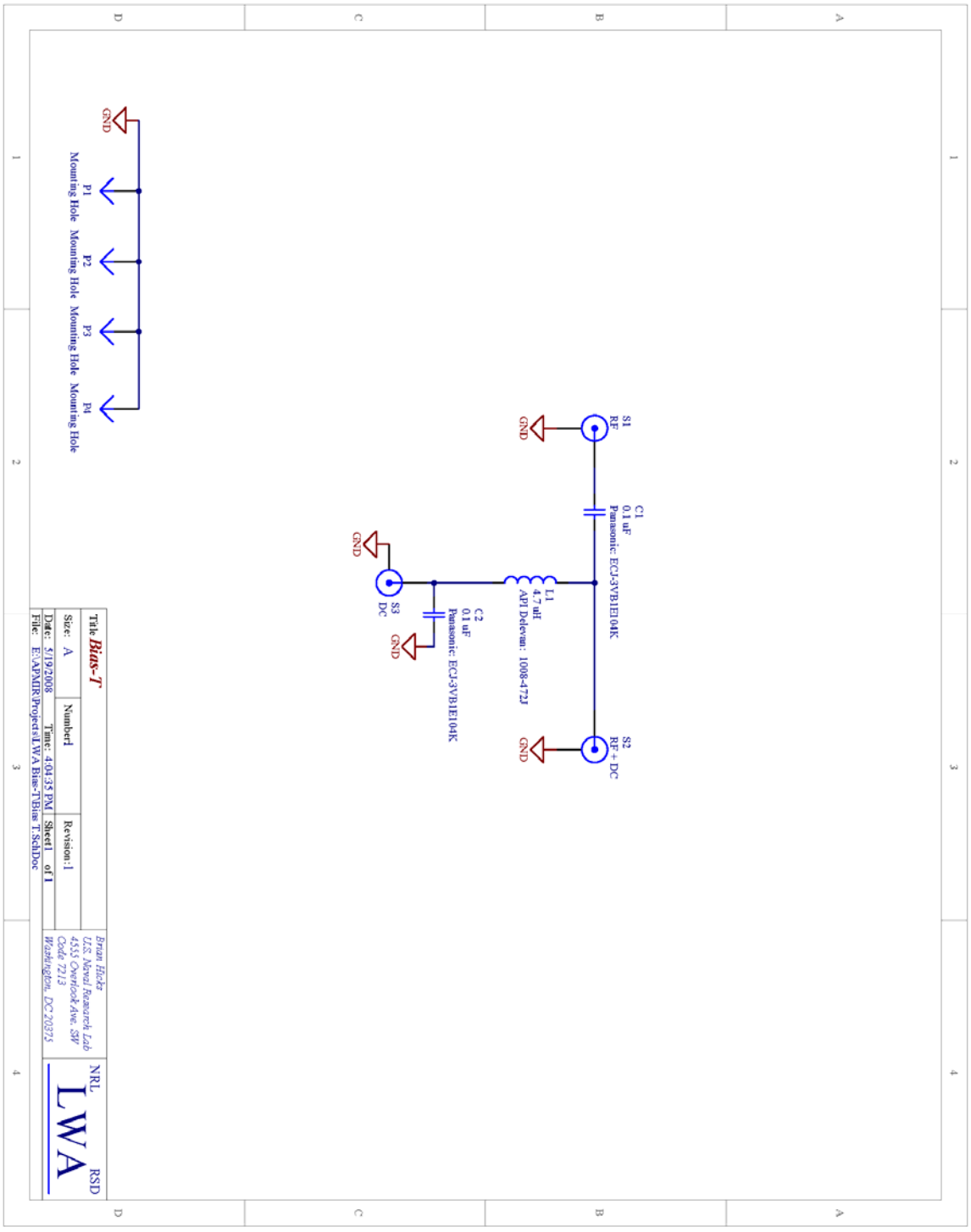


Figure 14 – Bias-T Schematic

IX. Schematics and Layouts (Continued)

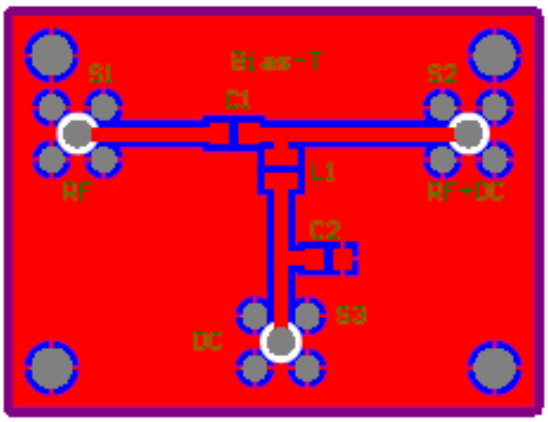


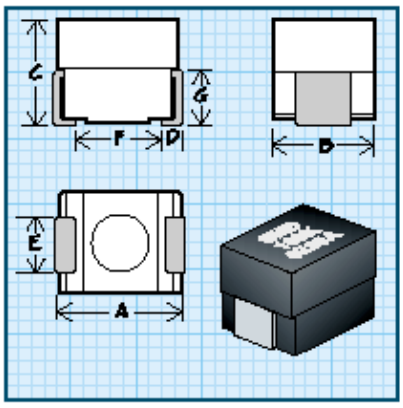
Figure 15 – Bias-T Evaluation PCB

Note: Active portion of circuit fits within an 8 x 10 mm rectangle.

X. Datasheets (L1 and C1)

Series 1008R / 1008

Unshielded Surface Mount Inductors



Physical Parameters

	Inches	Millimeters
A	0.095 to 0.115	2.41 to 2.92
B	0.085 to 0.105	2.16 to 2.66
C	0.075 to 0.095	1.91 to 2.41
D	0.010 to 0.030	0.26 to 0.76
E	0.040 to 0.060	1.02 to 1.52
F	0.060 (Ref. only)	1.52 (Ref. only)
G	0.045 (Ref. only)	1.14 (Ref. only)

Dimensions "A" and "C" are over terminals.

Weight Max. (Grams) 0.1

Operating Temperature Range –55°C to +125°C

Current Rating at 90°C Ambient 35°C Rise

Maximum Power Dissipation at 90°C
Phenolic: 0.169 W
Ferrite: 0.208 W

Packaging Tape & reel (8mm): 7" reel, 2000 pieces max.; 13" reel, 7000 pieces max.

Made In the U.S.A. ***Patent Protected***

DASH NUMBER	INDUCTANCE (µH)	TOLERANCE	Q MINIMUM	TEST FREQUENCY (MHz)	SRF MINIMUM (MHz)	DC RESISTANCE MAXIMUM (OHMS)	CURRENT RATING MAX. (mA)
SERIES 1008 PHENOLIC CORE							
-018M	0.0018	±20%	40	50	2700	0.050	1562
-022M	0.0022	±20%	40	50	2700	0.050	1562
-027M	0.0027	±20%	40	50	2700	0.050	1562
-033M	0.0033	±20%	40	50	2700	0.050	1562
-039M	0.0039	±20%	40	50	2700	0.050	1562
-047M	0.0047	±20%	40	50	2700	0.050	1562
-056M	0.0056	±20%	40	50	2700	0.050	1562
-068M	0.0068	±20%	40	50	2700	0.050	1562
-082M	0.0082	±20%	40	50	2700	0.050	1562
-100K	0.010	±10%	40	50	2700	0.050	1562
-120K	0.012	±10%	40	50	2450	0.058	1450
-150K	0.015	±10%	40	50	2200	0.064	1381
-180K	0.018	±10%	40	50	2000	0.070	1320
-220K	0.022	±10%	35	50	1800	0.080	1235
-270K	0.027	±10%	35	50	1625	0.090	1164
-330K	0.033	±10%	30	50	1450	0.100	1105
-390K	0.039	±10%	30	50	1335	0.110	1053
-470K	0.047	±10%	30	50	1220	0.120	1006
-560K	0.056	±10%	25	50	1110	0.170	847
-680K	0.068	±10%	25	50	1000	0.180	823
-820K	0.082	±10%	25	50	915	0.190	801
-101K	0.100	±10%	15	25	550	0.230	728
SERIES 1008 FERRITE CORE							
-121K	0.12	±10%	40	25	750	0.100	1225
-151K	0.15	±10%	40	25	650	0.110	1168
-181K	0.18	±10%	40	25	550	0.120	1119
-221K	0.22	±10%	40	25	450	0.135	1055
-271K	0.27	±10%	40	25	375	0.150	1000
-331K	0.33	±10%	40	25	300	0.165	954
-391K	0.39	±10%	40	25	250	0.180	913
-471K	0.47	±10%	40	25	215	0.210	846
-561K	0.56	±10%	40	25	195	0.230	808
-681K	0.68	±10%	40	25	175	0.260	760
-821K	0.82	±10%	40	25	140	0.300	708
-102J	1.0	±5%	30	7.9	125	0.320	685
-122J	1.2	±5%	30	7.9	100	0.430	591
-152J	1.5	±5%	30	7.9	92	0.500	548
-182J	1.8	±5%	30	7.9	76	0.720	457
-222J	2.2	±5%	30	7.9	70	0.800	433
-272J	2.7	±5%	30	7.9	62	0.880	413
-332J	3.3	±5%	30	7.9	60	0.950	396
-392J	3.9	±5%	30	7.9	57	1.20	354
-472J	4.7	±5%	30	7.9	47	1.35	334
-562J	5.6	±5%	30	7.9	44	1.54	312
-682J	6.8	±5%	30	7.9	35	2.00	274
-822J	8.2	±5%	30	7.9	33	2.16	264
-103J	10	±5%	30	7.9	28	2.50	245
-123J	12	±5%	30	2.5	24	3.50	207
-153J	15	±5%	30	2.5	21	4.00	194
-183J	18	±5%	30	2.5	19	5.00	173
-223J	22	±5%	30	2.5	17	6.00	158
-273J	27	±5%	30	2.5	15	7.00	146
-333J	33	±5%	30	2.5	13	8.00	135
-393J	39	±5%	30	2.5	12	9.00	125
-473J	47	±5%	30	2.5	11	10.00	120

Optional Tolerances: J = 5% H = 3% G = 2% F = 1%

***Complete part # must include series # PLUS the dash #**

For further surface finish information, refer to TECHNICAL section of this catalog.

RF INDUCTORS

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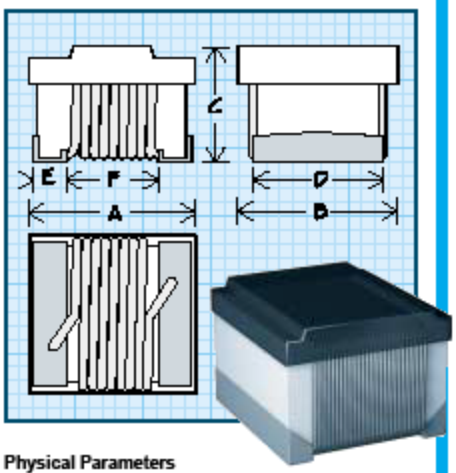
API Delevan American Precision Industries

Series WW1008R / WW1008

Wirewound Surface Mount Inductors



Physical Parameters

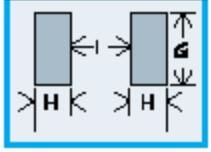
	Inches	Millimeters
A	0.115 Max.	2.92 Max.
B	0.110 Max.	2.79 Max.
C	0.080 Max.	2.03 Max.
D	0.080 (Ref. only)	2.03 (Ref. only)
E	0.020 (Ref. only)	0.50 (Ref. only)
F	0.060 (Ref. only)	1.52 (Ref. only)
G	0.100	2.54
H	0.040	1.01
I	0.050	1.27

Operating Temperature Range –40°C to +125°C

Inductance and Q tested on HP4291A using HP16193A test fixture, or equivalent

Packaging Tape & reel (8mm): 7" reel, 2000 pieces max.

LAND PATTERN DIMENSIONS



DASH NUMBER*	INDUCTANCE (nH) ±10%	INDUCTANCE TEST FREQUENCY (MHz)	Q MINIMUM	Q TEST FREQUENCY (MHz)	SRF MINIMUM (MHz)	DC RESISTANCE MAXIMUM (OHMS)	CURRENT RATING MAXIMUM (mA)
SERIES WW1008 CERAMIC CORE							
-5N6K	5.6	50	50	1500	4000	0.15	1000
-10NK	10	50	50	500	4100	0.08	1000
-12NK	12	50	50	500	3300	0.09	1000
-15NK	15	50	50	500	2500	0.11	1000
-18NK	18	50	50	350	2400	0.12	1000
-22NK	22	50	55	350	2400	0.12	1000
-24NK	24	50	55	350	1900	0.12	1000
-27NK	27	50	55	350	1600	0.13	1000
-33NK	33	50	60	350	1600	0.14	1000
-39NK	39	50	60	350	1500	0.15	1000
-47NK	47	50	65	350	1500	0.16	1000
-56NK	56	50	65	350	1300	0.18	1000
-59NK	59	50	65	350	1250	0.20	1000
-68NK	68	50	65	350	1300	0.20	1000
-75NK	75	50	60	350	1100	0.21	1000
-82NK	82	50	60	350	1000	0.22	1000
-101K	100	25	60	350	1000	0.56	650
-121K	120	25	60	350	950	0.63	650
-151K	150	25	45	100	850	0.70	580
-181K	180	25	45	100	750	0.77	520
-221K	220	25	45	100	700	0.84	500
-241K	240	25	45	100	650	0.88	500
-271K	270	25	45	100	600	0.91	500
-301K	300	25	45	100	585	1.00	450
-331K	330	25	45	100	570	1.05	450
-361K	360	25	45	100	530	1.10	470
-391K	390	25	45	100	500	1.12	470
-431K	430	25	45	100	480	1.15	470
-471K	470	25	45	100	450	1.19	470
-561K	560	25	45	100	415	1.33	400
-621K	620	25	45	100	375	1.40	300
-681K	680	25	45	100	375	1.47	400
-751K	750	25	45	100	360	1.54	360
-821K	820	25	35	100	350	1.61	400
-911K	910	25	35	50	320	1.68	380
-102K	1000	25	35	50	290	1.75	370
-122K	1200	7.9	35	50	250	2.00	310
-152K	1500	7.9	28	50	200	2.30	330
-182K	1800	7.9	28	50	160	2.60	300
-222K	2200	7.9	28	50	160	2.80	280
-272K	2700	7.9	22	25	140	3.20	290
-332K	3300	7.9	22	25	110	3.40	290
-392K	3900	7.9	20	25	100	3.60	260
-472K	4700	7.9	20	25	90	4.00	260
-562K	5600	7.9	16	7.9	40	4.00	240
-682K	6800	7.9	18	7.9	40	4.90	200
-822K	8200	7.9	18	7.9	25	6.00	170
-103K	10000	2.5	18	7.9	20	9.00	150
-123K	12000	2.5	18	7.9	18	10.50	130
-153K	15000	2.5	18	7.9	15	11.50	120

Optional Tolerances: J = 5% G = 2%
(5.6nH Min. Tolerance is ±5%)

***Complete part # must include series # PLUS the dash #**

For further surface finish information, refer to TECHNICAL section of this catalog.

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API Delevan American Precision Industries

Multilayer Ceramic Capacitors (For General Electronic Equipment)

Series: **ECJ**

■ Features
- Small size and wide capacitance range
- High humidity resistance and long life
- Excellent solderability and resistance to soldering heat
- Low inductance (ESL) and excellent frequency characteristics
- RoHS compliant

■ Recommended Applications
- Class 1 (T.C. Type)
  Tuned circuits, and filter circuitry, where low loss and high stability of capacitance and high insulation resistance is required
- Class 2 (Hi-K Type)
  Coupling and By-passing

■ Handling Precautions
See Page 48 to 53

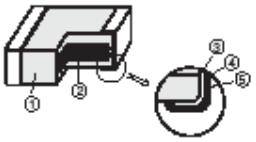
■ Packaging Specifications
See Page 45, 46, 56

■ Explanation of Part Numbers

1	2	3	4	5	6	7	8	9	10	11	12	
E	C	J	Z	E	B	1	A	1	0	3	K	(Example)

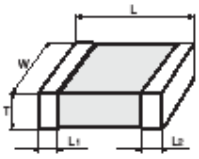
- 1 2 3: Product Code (ECJ:Multilayer Ceramic Chip Capacitors)
- 4: Size Code
- 5: Packaging Style Code
- 6: Temperature Characteristic Code
- 7 8: Rated Voltage Code
- 9 10 11: Nominal Capacitance
- 12: Capacitance Tolerance Code

■ Construction



No	Name	
①	Ceramic dielectric	
②	Internal electrode	
③	Terminal electrode	Substrate electrode
④		Intermediate electrode
⑤		External electrode

■ Dimensions in mm (not to scale)



Size Code	Size (EIA)	L	W	T	L_1, L_2
Z	0201	0.60±0.03	0.30±0.03	0.30±0.03	0.15±0.05
0	0402	1.00±0.05	0.50±0.05	0.50±0.05	0.2±0.1
1	0603	1.6±0.1	0.8±0.1	0.8±0.1	0.3±0.2
2	0805	2.0±0.1	1.25±0.10	0.6±0.1	0.50±0.25
				0.85±0.10	
				1.25±0.10	
		2.00±0.15	1.25±0.15	1.25±0.15	

■ Packaging Styles and Standard Packaging Quantities

Quantity (Taping: pcs./reel)

Packaging Style Code	Packaging Styles \ Size / Thickness (mm)		0201 T=0.3	0402 T=0.5	0603 T=0.8	0805 T=0.6	0805 T=0.85	0805 T=1.25
E	φ180 reel	Paper taping (Pitch: 2 mm)	15,000	10,000	—	—	—	—
V	φ180 reel	Paper taping (Pitch: 4 mm)	—	—	4,000	5,000	4,000	—
F	φ180 reel	Embossed taping (Pitch: 4 mm)	—	—	—	—	—	3,000

φ330 reel and bulk case type : Please contact us

■ Temperature Characteristics

● Class 1

Temperature Characteristic Code	Temperature Characteristics			Temp. Coeff. (ppm/°C)	Rate of Capacitance change at each Temperature (%)			
					−25 °C		85 °C	
					max.	min.	max.	min.
C	CΔ	≧10 pF	CG	0± 30	0.33	−0.14	0.20	−0.20
		≧4 pF	CH	0± 60	0.49	−0.27	0.39	−0.39
		3 pF	CJ	0±120	0.82	−0.54	0.78	−0.78
		≦2 pF	CK	0±250	1.54	−1.13	1.63	−1.63
G	SL			+350 to −1000	—	—	2.28	−6.50

Temperature coefficient: calculated between 20 °C to 85 °C
For applicable "temperature characteristics", see the lists of standard products on page 13 to 19.

● Class 2

Temperature Characteristic Code	Temperature Characteristics	Capacitance Change	Measurement Temperature Range	Reference Temperature
B	B	±10 %	−25 to 85 °C	20 °C
	X7R	±15 %	−55 to 125 °C	25 °C
	X5R	±15 %	−55 to 85 °C	25 °C
F	F	+30, −80 %	−25 to 85 °C	20 °C
	Y5V	+22, −82 %	−30 to 85 °C	25 °C

For applicable "temperature characteristics", see the lists of standard products on page 13 to 19.

■ Rated Voltage

Code	1H	1E	1C	1A	0J
Rated Voltage	DC 50 V	DC 25 V	DC 16 V	DC 10 V	DC 6.3 V

■ Nominal Capacitance

Ex	0R5	010	100	104
Nominal Capacitance	0.5 pF	1 pF	10 pF	100,000 pF (0.1 μF)

■ Capacitance Tolerance

Class	Temperature Characteristics			Tol. Code	Capacitance Tolerance
1	CΔ, SL	Capacitance range	C ≦ 5 pF	C	±0.25 pF
			C ≦10 pF	D	±0.5 pF
			C =10 pF	F	±1 pF
			C >10 pF	J	±5 %
				K	±10 %
2	B, X7R, X5R			K	±10 %
				M	±20 %
	F, Y5V			Z	+80, −20 %