National Institute of Justice Grant 2005-IJ-CX-K018
(“A Low Cost All-Band All-Mode Radio for Public Safety”)

Final Report

S.W. Ellingson*

December 30, 2008

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1 Executive Summary

This final report concludes the project “A Low Cost All-Band All-Mode Radio for Public Safety,” performed under Grant No. 2005-IJ-CX-K018 from the National Institute of Justice of the U.S. Dept. of Justice. The goal of this project was to develop and demonstrate a low-cost radio which can operate in all bands and all modes relevant to public safety operations in the United States. A quad chart summarizing the project is shown in Figure 1.

Over the course of this project, we studied several design approaches, including prototyping and evaluation of working hardware. We settled on a design using a direct conversion architecture. Direct conversion is an obvious option for low cost radios with very large multiband tuning range, but is prone to problems which make the demanding requirements of Public Safety applications very difficult to achieve. Significant improvement in the performance of direct conversion has become possible with the development of a new CMOS RF integrated circuit (RFIC) announced by Motorola in June 2007. With cooperation and technical support from Motorola, we have used this transceiver chip as the basis for our radio. A remaining obstacle was the problem of how to interface a single, conventional antenna to the RFIC while providing sufficient isolation between bands. For this, we developed an RF multiplexer which is jointly optimized with respect to the antenna impedance and to the existing external noise environment in such a way that acceptable receive sensitivity can be achieved despite large impedance mismatch with the antenna. The completed radio tunes 138–174 MHz, 220–222 MHz, 406–512 MHz, and 764–900 MHz, and is also capable of operation in the 2.4 GHz and 4.8 GHz bands with simple extensions to the design. The radio as implemented supports only analog FM, however all baseband processing is implemented on a large FPGA upon which any mode, or combination of modes, could be implemented as a firmware upgrade. Because the baseband processing is implemented on an FPGA, as opposed to a microprocessor or general purpose computer, the design is very simple and inexpensive, yet extremely rapid reconfiguration as well as simultaneous processing of multiple channels – difficult to achieve in conventional microprocessor-based designs – is possible.

Our actual “pile of parts” cost for the completed prototype was about $3900. If this radio were to be produced in quantities greater than 10 or so, there would be at least $1200 savings in the cost of printed circuit boards alone, plus another $1200 that could be saved by replacing the FPGA evaluation board used in our prototype with a simpler custom board containing only the FPGA chip. A few other factors associated with economies of scale account for an additional $300 reduction. Although much additional engineering development would be necessary for a production model, we estimate that the corresponding “pile of parts” cost for a production model with capabilities similar to our prototype would be roughly $1200.

One of the principal goals of this project was to disseminate technical findings, including design data, as broadly as possible; especially with respect to manufacturers of public safety radio equipment. Our principal method for this is the project web site,¹ which provides open access to technical memos and associated design files (including software and CAD data), papers, presentations, and other documents generated as a result of this project. We have also worked directly with Motorola (as discussed above), and briefed Tyco Electronics (resulting in a new project on design of multiband portable radios) and E.F. Johnson Corp.

¹http://www.ece.vt.edu/swe/chamrad/
Figure 1: Quad chart summary of project (from the April 2008 NIJ TWG meeting).

Multiband / Multimode Radio (2005-IJ-CX-K018)
FA1 (Next Generation Interoperable Voice Communications)
S.W. Ellingson (ellingson@vt.edu)
Project End Date: September 30, 2008

Technology
Low-cost radio capable of operation over a large range of frequency bands now in use for public safety applications.

Vendor/Research Program Contributions
- Using RF Integrated Circuit (RFIC) transceiver technology developed by Motorola Research Laboratories
- Description of RFIC: Cafaro et al., Proc. IEEE RFIC Sym., June 2007
- In communication with Tyco Electronics (M/A-COM) and EF Johnson
- All design information and other products from this project freely available to anyone via project web site (see above right)

VT Transceiver Board using Motorola-Provided RFIC
4 RX Paths, 3 TX Paths
100-2500 MHz tuning
6.25 kHz – 10 MHz BW

Key Deliverables
- Phase I Rep. (TR#15, Oct 1, 2006)
- Phase II Rep. (TR#23, Oct 5, 2007)
- Phase IV Rep. (due Jul 1, 2008)
- Final Rep. (due Oct 1, 2008)
- Public demo scheduled for 2008 Wireless @ Virginia Tech Annual Symp. & Wireless Summer School
- Publications:
  - Article in MissionCritical Communications, March 2007
  - Project Web Site (incl. all deliverables): http://www.ece.vt.edu/swe/chamrad/ (Currently 25 technical reports)

Law Enforcement Impact
- Interoperability with multiple networks simultaneously without prior coordination or infrastructure-based interoperability devices such as cross-band repeaters
- Portable battery-powered prototype system (see above right) available for demonstration beginning Summer 2008. (Field evaluation by users would require additional effort on packaging)
- Challenges Remaining:
  - Antenna size & integration
  - Increasing transmit power
  - Technology transfer
2 Project Summary and Accomplishments

This final report concludes the project “A Low Cost All-Band All-Mode Radio for Public Safety,” performed under Grant No. 2005-IJ-CX-K018 from the National Institute of Justice of the U.S. Dept. of Justice. The primary goal of this project was to develop and demonstrate a radio which can operate in all bands and all modes relevant to public safety operations in the United States. The motivation behind this project, including a discussion of the associated user requirements, can be found in Section 2 of the Phase I technical report, which is included in its entirety as Appendix D of this report.

This project has culminated in the development and demonstration of a prototype radio. A brief description of the radio and associated findings can be found in the presentation slides in Appendix C of this report. Elaboration on these findings and conclusions are reported below. Complete documentation of all aspects of the project are available on the project web site. For convenience, Appendix A provides a list of all technical memos completed as part of this project, and selected technical memos documenting the final design and containing key findings and conclusions are reproduced in the appendices of this report.

This following is a summary of the principal outcomes of the project:

- Analysis, design, and development leading to a prototype multiband/multimode radio. A summary description of the radio is given in Appendix F (“Phase III/IV Report”) with design details given in Appendix H. The rationale behind selection of this architecture is given in Section 3 of Memo 23 (Appendix E).

- As part of our efforts to develop the radio, we explored the use of optimized RF multiplexers for connecting small conventional antennas to multiband transceivers. Unlike conventional approaches, this approach requires no switches or tuning, yet provides simultaneous access to very large fractional bandwidths below 1 GHz. This is documented in Memo 25 (included in this report as Appendix G) and is the topic of a Ph.D. dissertation, currently in preparation.

- Analysis, design, and development of alternatives to the above radio. We carefully studied and documented alternative approaches to RF hardware (Memos 10 and 16; also Sections 2.1 and 2.2 of Memo 23/Appendix E) and digital/baseband processing (Memos 1–3, 5–7, 9, 11, 12, 14, and 18; also Section 2.3 of of Memo 23/Appendix E). In particular, we investigated the use the U.S. DOD “Software Communications Architecture” (SCA) (Memos 1, 3, 5, 6, 9, and 14), as well as a reduced-cost/complexity approach using a combination of FPGAs and embedded processors running Linux (Memos 2, 7, 11, 12, and 18). We designed and tested hardware and software based on these approaches. Although these approaches were not adopted in our radio, they provided useful information and the designs and subsequent findings may find application in other efforts.

- This project has led to collaborations with Motorola and Tyco Electronics. We have been working with Motorola Research Laboratories since January 2007 on the application of Motorola’s RFIC technology to low-cost multiband/multimode radio. In our new collaborative project with Tyco Electronics, we will study design options for future multiband portable radios.

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2http://www.ece.vt.edu/swe/chamrad/
3This dissertation will be added to the project web site upon completion.
An extensive program of outreach and dissemination has been conducted, with outcomes documented in Appendix B.

The remainder of this report is organized as follows.

- Appendix A ("List of Technical Reports") provides a complete index of technical reports written during this project.
- Appendix B ("Outreach and Dissemination") documents the outcomes of our program of outreach and dissemination.
- Appendix C ("Project Briefing") is a recent (October 2008) presentation on the project, which may be useful as quick introduction and overview.
- Appendices D and E are the complete contents of the Phase I and II technical reports, respectively. These are provided as documentation of various aspects of the project as discussed above.
- Appendix F ("Phase III/IV Report") is the complete contents of Technical Memo 26, a paper recently presented at Software Defined Radio (SDR) ’08 (Washington DC, October 2008).
- Appendix G is the complete contents of Technical Memo 25 (a paper presented at the IEEE Int’l Antennas & Propagation Symp., San Diego, CA, July 10, 2008), which describes our approach to antenna-receiver integration using an RF multiplexer.
- Appendix H ("Design Details") is the complete contents of Technical Memos 28–31, which together document the latest design of the radio developed in this project.

3 Acknowledgments and Disclaimer

This project was supported by Award No. 2005-IJ-CX-K018 awarded by the National Institute of Justice, Office of Justice Programs, U.S. Department of Justice. The opinions, findings, and conclusions or recommendations expressed in this publication/program/exhibition are those of the author(s) and do not necessarily reflect the views of the Department of Justice.

Virginia Tech contributors to this project include Prof. J.H. Reed; post-doctoral researchers C.R. Anderson and M. Robert; and students P. Ballister, S.M. Shajedul Hasan, M. Harun, K. Hurst, K. Lee, Q. Liu, J.H. Oh, R. Thandee, T. Tsou.

We are grateful to Neiyer Correal, Bob Stengel, and Gio Cafaro of Motorola for providing RFIC chips and evaluation boards, as well as extensive and patient technical assistance.
A List of Technical Reports

The following is a list of all technical reports ("memos") completed as part of this project. All reports are available via the project web site.\(^4\) Reports are listed in chronological order.


\(^4\)http://www.ece.vt.edu/swe/chamrad


B Outreach and Dissemination

The following is a list of efforts towards outreach and dissemination of results in this project.

- **Papers in journals subject to peer review:**
  

- **Papers presented in technical conferences subject to peer review:**
  
  

- **Articles in trade magazines:**
  

- **Presentations in trade conferences:**
  
  
  
  
  
  

- **Presentations to industry representatives:**
  
  

• Demonstrations:
  – *Wireless @ Virginia Tech Annual Symposium*, Blacksburg, VA, Jun 4-6, 2008.

• Short courses based on developments from this project:
  – S.W. Ellingson, *Design Techniques for Multiband/Multimode Radio*, presented at the *Wireless @ Virginia Tech Annual Symposium*, Blacksburg, VA, Jun 4-6, 2008; lecture notes available as Technical Memo 27 on the project web site.

• Website: http://www.ece.vt.edu/swe/chamrad.
C Project Briefing

The following presentation, delivered at the October 2008 technical meeting of the Software Defined Radio Forum in Washington, D.C., is provided as a brief introduction and overview of the project. See Appendix F for the paper from which this presentation was derived.
Multiband Public Safety Radio using a Multiband RFIC with an RF Multiplexer-based Antenna Interface

S.M. Hasan and S. W. Ellingson

Wireless at Virginia Tech
Bradley Dept. of ECE, Virginia Tech,
Blacksburg, VA 24060

October 28, 2008
Motivation (1/2)

Frequency Bands:
- VHF LO (25-50 MHz)
- VHF (138-174 MHz)
- 220 MHz
- UHF (406-512 MHz)
- 700 MHz P.S.
- 800 MHz P.S.
- Cellular & PCS
- 2.4 GHz ISM
- 4.9 GHz P.S.

Combine Many Radios into One*
At least 13 bands relevant to Public Safety
x Many channels per band = A lot of radios!
(*Above figure is just a functional description.)

Goal: Seamless Interoperability

Developing a prototype radio capable of operation over a large range of frequency bands now in use for public safety applications.

Multiband/Multimode Radio
Hasan / Ellingson – October 28, 2008
Motivation (2/2)

For Multiband Multimode Radios (MMR)s

- **Superhet Design**
  - Power Hungry/ Large/ Complex/ Expensive

- **Direct Conversion Design**
  - Low Cost/ Small Size/ Low Power/No IF Filter
  - **Cons**: I/Q imbalance, In band 1/f noise from LO, IP2, Initial BPF

Problems with direct conversion design can now be largely mitigated by:

- Implementing design to be robust to variations
- Exploiting availability of nearby logic to enable radio to tweak chip as needed
- 1/f noise is mitigated by using the combination of DDS and chopping
System Diagram of the Prototype
Motorola Direct Conversion RFIC

Specs (Verified by VT in Independent Testing)

- 5 RX Paths (1 output)
- 3 TX Paths (1 input)
- RX F ~ 5 dB
- RX IIP₂ ~ +60 dBm
- RX IIP₃ ~ −5 dBm
- 90 nm CMOS
- No inductors
- QFN-100
- < 400 mA @ 2.5V (RX+TX)

Tunes 100 - 2500 MHz (continuous)
- BW: 4.25 kHz – 10 MHz (many steps)
- Sideband Rejection ~ 40 dB, up to 60 dB
- Internal DDSs for LO generation
- Excellent mitigation of 1/f noise

Advantages of RFIC-Based Direct Conversion in this Project

- **Scalable** – Same architecture works for reduced or increased number of simultaneous channels/bands (just add/remove chips)

- **Reduced power (extended battery life)** – lower power/channel and unneeded RFICs (or RFIC sections) can be shut down.

- Increased number of channels can be monitored simultaneously, even across bands: Scanner-like capability, “White space” seeker(s) for frequency-agile cognitive radio

- **Con**: Optimization requires calibration and tweaking of many parameters (over a low-bandwidth SPI serial port)
VT Transceiver Board

**Receiver Section:**
Avg. Gain: 48 dB
I/P 1dB Comp. Pt: -26 dBm
Sideband Rejection: 29 dB
Power: 1.1 W (10V@0.11A)

**Transmitter Section:**
Avg. O/P Power: -4 dBm
O/P 1 dB Comp. Pt: -5 dBm
Sideband Rejection: 22 dB
Power: 1.7 W (10V@0.17A)

No parameter optimization in the RFIC has been performed

- 4-Band Transceiver Board
- Implemented on a 4-layer PCB
- About $100 in parts to implement, excluding PCB.
Antenna Interfacing Idea?

- Sensitivity depends on signal to noise ratio
- External noise can be very strong in practical scenarios, especially at low frequencies (below ~400 MHz)
- If \( \gamma \) is large, additional effort to minimize \(|\Gamma|\) or \( T_{FE} \) will have little effect on sensitivity
- If acceptable \( \gamma \) can be achieved for a poor \(|\Gamma|\), improvements in \(|\Gamma|\) are actually counterproductive, since this complicates the design

Our idea is to design a multiplexer, which may be poorly matched with the antenna impedance, in such a way that the front end is dominated by the external noise and provide acceptable sensitivity

\[
\gamma = \eta (1 - |\Gamma|^2) \frac{T_{ext}}{T_{FE}}
\]

Reflection co-efficient,

\[
\Gamma = \frac{Z_{in} - Z_{ant}}{Z_{in} \cdot Z_{ant}}
\]
Thevenin model of antenna impedance

\[ Z_{\text{ant,Monopole}} = \frac{1}{2} Z_{\text{ant,Dipole}} \]

Thevenin model of antenna

\[ C_1 = \frac{12.674h}{\log(2h/a) - 0.7245} \text{ pF} \]
\[ C_2 = 2h \left\{ \frac{0.89075}{[\log(2h/a)]^{0.8006}} - 0.861 - 0.02541 \right\} \text{ pF} \]
\[ L = 0.2h \left\{ [1.4813 \log(2h/a)]^{1.012} - 0.6188 \right\} \text{ uH} \]
\[ R = 0.41288 [\log(2h/a)]^2 + 3.70377 (2h/a)^{-0.02389} - 3.63704 \text{ kOhm} \]

Antenna Model (2/2)

Circuit model & impedance for a 20 cm monopole of 5 mm radius
# External ("Environmental") Noise

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>Quiet Rural</th>
<th>Rural</th>
<th>Residential</th>
<th>Business A/B</th>
<th>Celestial$^1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-30</td>
<td>$3.81 \times 10^{25}$</td>
<td>$2.53 \times 10^{26}$</td>
<td>$8.54 \times 10^{26}$</td>
<td>$2.30 \times 10^{27}$</td>
<td>$1.07 \times 10^{23}$</td>
</tr>
<tr>
<td></td>
<td>2.86</td>
<td>2.77</td>
<td>2.77</td>
<td>2.77</td>
<td>2.52</td>
</tr>
<tr>
<td>30-100</td>
<td></td>
<td>$2.53 \times 10^{26}$</td>
<td>$8.54 \times 10^{26}$</td>
<td>$2.30 \times 10^{27}$</td>
<td>$1.07 \times 10^{23}$</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>2.77</td>
<td>2.77</td>
<td>2.77</td>
<td>2.52</td>
</tr>
<tr>
<td>100-130</td>
<td></td>
<td>$2.53 \times 10^{26}$</td>
<td>$8.54 \times 10^{26}$</td>
<td>$2.30 \times 10^{27}$</td>
<td>$1.07 \times 10^{23}$</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>2.77</td>
<td>2.77</td>
<td>2.77</td>
<td>2.52</td>
</tr>
<tr>
<td>130-250</td>
<td></td>
<td>$2.53 \times 10^{26}$</td>
<td>$8.54 \times 10^{26}$</td>
<td>$7.46 \times 10^{14}$</td>
<td>$1.07 \times 10^{23}$</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>2.77</td>
<td>2.77</td>
<td>1.23</td>
<td>2.52</td>
</tr>
<tr>
<td>250-900</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>900-3000</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td></td>
<td>-</td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

Mean noise temperature,
\[ T = af^{-b} \text{ [K]} \]

External Noise limits receiver’s sensitivity if -
\[ T_{ext} > T_{FE} \]

Standard deviation with respect to location


---

1. Add 2.7 K to account for CMB.
2. Decile values not available from [5], using \( D_1 = D_4 = 6.8 \text{ dB as for "Rural".} \)
3. Decile values not available from [5], using \( D_1 = D_4 = 8.4 \text{ dB as for "Business B".} \)
4. Varies over about 2 dB depending on time of day; see [6].

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Multiband/Multimode Radio
Hasan / Ellingson – October 28, 2008

Wireless @ Virginia Tech
This is the noise figure required of an amplifier attached to an antenna if the output is to be dominated by external noise by a factor of 10 in 90% of locations of the indicated type.

Optimum in the sense that any lower noise figure does not significantly increase sensitivity (only cost).

These particular results assume lossless, perfectly matched antenna with no ground loss.

- Prevents over-specifying receiver NF
- Can be interpreted as a loosened constraint
Multiplexer Architecture

Transducer Power Gain (TPG):

TPG is defined as the ratio of power delivered by a matching network to a load, to the power delivered to perfectly matched load directly from the antenna.
Results: Before Optimization

- **Solid Line:** Antenna Impedance is assumed as constant 50Ω
- **Dotted Line:** Antenna Impedance is assumed as TTG impedance
Results: After Optimization

Design Criteria:

(1) The ratio of external (unavoidable) noise to internally generated noise at the output of a receiver front end should be large

(2) The TPG should be reasonably flat over the passband

- Channels are jointly optimized using GENESYS
- Channel 1 & 2 are optimized to achieve maximum flatness
- Channel 3 & 4 are optimized to get maximum TPG
## Results: Noise Dominance

"External noise dominance" in VHF-High and 220 MHz bands

### Component Values

<table>
<thead>
<tr>
<th>Component</th>
<th>Channel 1 Before</th>
<th>Channel 1 After</th>
<th>Channel 2 Before</th>
<th>Channel 2 After</th>
<th>Channel 3 Before</th>
<th>Channel 3 After</th>
<th>Channel 4 Before</th>
<th>Channel 4 After</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1 (nH)</td>
<td>377.1</td>
<td>290.6</td>
<td>1357.4</td>
<td>1322.5</td>
<td>111.2</td>
<td>82.5</td>
<td>114.9</td>
<td>81.1</td>
</tr>
<tr>
<td>C1 (pF)</td>
<td>2.8</td>
<td>6.9</td>
<td>0.4</td>
<td>0.4</td>
<td>1.1</td>
<td>1.1</td>
<td>0.3</td>
<td>0.3</td>
</tr>
<tr>
<td>L2 (nH)</td>
<td>9.7</td>
<td>7.6</td>
<td>1.3</td>
<td>1.3</td>
<td>3.1</td>
<td>3.1</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>C2 (pF)</td>
<td>108.7</td>
<td>136.1</td>
<td>391.4</td>
<td>389.4</td>
<td>39.0</td>
<td>39.0</td>
<td>42.8</td>
<td>42.8</td>
</tr>
<tr>
<td>L3 (nH)</td>
<td>561.6</td>
<td>402.9</td>
<td>2021.9</td>
<td>2101.2</td>
<td>173.4</td>
<td>173.4</td>
<td>182.0</td>
<td>182.0</td>
</tr>
<tr>
<td>C3 (pF)</td>
<td>1.9</td>
<td>2.6</td>
<td>0.3</td>
<td>0.3</td>
<td>0.7</td>
<td>0.7</td>
<td>0.2</td>
<td>0.2</td>
</tr>
<tr>
<td>L4 (nH)</td>
<td>9.7</td>
<td>8.3</td>
<td>1.3</td>
<td>1.2</td>
<td>3.1</td>
<td>3.1</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>C4 (pF)</td>
<td>108.7</td>
<td>125.1</td>
<td>391.4</td>
<td>437.5</td>
<td>39.0</td>
<td>39.0</td>
<td>42.8</td>
<td>42.8</td>
</tr>
<tr>
<td>L5 (nH)</td>
<td>377.1</td>
<td>207.2</td>
<td>1357.4</td>
<td>1301.4</td>
<td>112.2</td>
<td>112.2</td>
<td>114.9</td>
<td>114.9</td>
</tr>
<tr>
<td>C5 (pF)</td>
<td>2.8</td>
<td>5.1</td>
<td>0.4</td>
<td>0.4</td>
<td>1.1</td>
<td>1.1</td>
<td>0.3</td>
<td>0.3</td>
</tr>
</tbody>
</table>

**Multiband/Multimode Radio**

Hasan / Ellingson – October 28, 2008
Multiplexer in the Prototype

Impedance of actual antenna used (ANT-433-CW)

Multiplexer using ANT-433-CW

$5 Antenna from Digikey

Multiband/Multimode Radio
Hasan / Ellingson – October 28, 2008
RF Front End Board

VT RF Front End Board

➢ RF Multiplexer to interface with Antenna
➢ Low Noise Amplifier
➢ Additional Filters
➢ Variable Attenuators to control gain
➢ 4 Layer PCB
➢ About $200 in parts to implement
Digital Signal Processing

VT ADC / DAC / LO Synthesizer Board
- ADC/DAC: 130 mA @ 9V, running 4 MSPS
- Implement on a 4-layer PCB
- ADC ~ $21 (1k), DAC ~ $10 (1k)

EP2S60 Stratix II DSP development board
- Altera Stratix II FPGA
- Audio CODEC
- Firmware is written in Verilog HDL
- This FPGA is extremely overkill for this application

Multiband/Multimode Radio
Hasan / Ellingson – October 28, 2008
User Interface & Audio Board

Gumstix LCD pack
- 600 MHz Intel PXA27X Processor
- Samsung touchscreen LCD
- X-Window Operating System in 2GB SD card

Audio Board
- Connect standard handheld Mic & Spkr
- Audio amplifiers for MIC & Speaker
- Supplies PTT signals to FPGA
Prototype

Multiband/Multimode Radio
Hasan / Ellingson – October 28, 2008

- 138-174 MHz
- 220-222 MHz
- 406-512 MHz
- 764-900 MHz

Motorola RFIC Ver. 4
4 MSPS baseband
ADC/DAC
No μP; Instead completely implemented in FPGA

Status (10/23/08)
RF Mux: Works
RFIC Board: Works
ADC/DAC: Works
Baseband: Analog FM Only
CODEC: Works
PTT: Works

Three board stack integrates antenna, RF Mux, transceiver, RFIC, ADC / DAC, ref. freq. synthesizer

Off-the-shelf antenna
Touchscreen
Audio I/F
Ethernet
Battery underneath
Altera EP2S60 FPGA Board
Summary Remarks

- RF multiplexer optimized to antenna impedance with external noise dominance constraint, allows good performance in multiple bands

- Principal advantage over reconfigurable matching techniques: Simultaneous access to multiple bands

- Good result with 20 cm 5 mm rod antenna, but less good performance with commercial (433 MHz) antenna
  - Co-design of antenna and multiplexer may be advantageous

- Performance of RFIC-based design is still a bit short of public safety selectivity and dynamic range requirements

- Challenges:
  - Requires amplifier with a little better NF than commonly used
  - Realizing small filter footprint
  - Building a good user interface to control the whole radio
Thanks!

Acknowledgements:
Motorola: G. Cafaro, B. Stengle, N. Correal
Mahmud Harun (student)
Rithirong Thandee (student)
Qian Liu (Student)

Project Web Site:
http://www.ece.vt.edu/swe/chamrad/

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U.S. Dept. of Justice
National Institute of Justice
Grant 2005-IJ-CX-K018
D Phase I Report

This appendix is a complete copy of the Phase I technical report, which documents various aspects of the project.
Phase I Technical Report

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October 1, 2006
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1 Introduction

This report summarizes the efforts performed in Phase I of the project “A Low Cost All-Band All-Mode Radio for Public Safety,” performed under Grant No. 2005-IJ-CX-K018 from the National Institute of Justice of the U.S. Dept. of Justice. The overall goal of this project is to develop and demonstrate a radio which can operate in all bands and all modes relevant to public safety operations in the U.S., with a special emphasis on cost. This project is documented via the project web site [1], including a recent overview presentation [2].

In this phase of the project, we have investigated the problem and developed some preliminary solutions with no special emphasis on cost. In subsequent stages of the project, we will consider alternative approaches, attempt to identify and quantify cost-performance tradeoffs, and demonstrate a prototype.

The following technical memoranda were generated during this phase of the work, and should be considered intrinsic to this technical report:

This report is organized as follows. Section 2 describes the interoperability problem in public safety communications, and describes the manner of solution which this work intends to provide. Section 3 summarizes the work accomplished to date, as described in the technical memoranda listed above. Section 4 presents a “strawman” design, which represents our current preferences as to the implementation of the radio.
2 The User-Based Approach to Interoperability in Public Safety Wireless Communications

This section describes the interoperability problem in public safety communications, and describes the manner of solution which this work intends to provide. This section is organized as follows. Section 2.1 provides a general description of public safety wireless communications, the frequencies of interest, and the nature of the interoperability problem. Section 2.2 describes “network-based” interoperability, which is in common use in various forms today. Section 2.3 describes “user-based” interoperability, in which it is the user radios, as opposed to the network infrastructure, which provide interoperability. Section 2.4 describes the implementation of user-based interoperability using software-defined radio (SDR) technology. Section 2.5 addresses the question of why military SDRs are probably not an appropriate avenue to user-based interoperability in public safety applications. Section 2.6 summarizes this discussion and itemizes the pros and cons of the proposed solution: a user-based interoperability radio based on commercial SDR technology.

2.1 The Interoperability Problem

Wireless communications are an essential and expansive aspect of public safety operations. An introduction to public safety wireless communications is provided in [17]. Recently, the SAFECOM program of the U.S. Dept. of Homeland Security released a document which provides a comprehensive description of the use of wireless communications in public safety operations, and a summary of requirements [18].

One way to describe public safety communications is in terms of the frequency bands which are used, and the modes of communication that are used in each band. This summarized in Table 1. Modes include:

- TIA-603 analog FM voice [21]
- APCO Project 25 (P25) digital voice and data [22, 23]
- TIA-902 wideband data [24, 25, 26]
- Various existing commercial wireless modes, including cellular, PCS, and IEEE 802-series wireless protocols.

In the report of the National Task Force on Interoperability [27], the public safety community identified incompatible equipment, limited/fragmented radio spectrum, and a profusion of proprietary systems as some of the key problems that prevent organizations from conducting critical public safety radio communications in both routine operations and in emergencies including acts of terrorism and natural disasters. The root cause of much of this difficulty is the “stove-piped” nature of communications networks currently used by public safety agencies. That is, whenever a public safety organization has the opportunity to upgrade or replace an existing radio system, it
Table 1: Bands of interest to the public safety community. Compiled from [2, 10, 19, 20]. RL = Reverse link (mobile to base), FL = forward link (base to mobile).

must typically choose a single band and mode, which compromises interoperability with organizations which have chosen differently.

The ultimate solution to this problem is likely to be through a synthesis of three technologies: (1) open standards, (2) software-defined radio (SDR), and (3) cognitive radio. As illustrated in Figure 1, open standards such as P25 may eventually replace proprietary standards, leading to a situation in which the current long list of incompatible modes is replaced with a reduced number of straightforwardly-interoperable modes. SDR technology enables a radio to change its mode or other operating parameters on-the-fly, facilitating the easy and perhaps even real-time adoption of standards different from that which the radio had originally been intended to use [28]. Cognitive radio technology allows radios to independently sense their environment and collaborate with other radios to optimally choose frequencies, modes, and other operating parameters automatically [29]. Employed together, these technologies may one day lead to radio networks that “just work” – i.e., which dynamically make optimal choices of band and mode in response to changing conditions, and do this in a manner which is transparent to the users.

Unfortunately, this goal appears to be at least a decade or more away. Barriers include the very long time required to develop and adopt standards, the immature state of SDR and cognitive radio technology, the very long time required to accommodate SDR and cognitive radio concepts in the existing regulatory structure, the cost and time required to replace equipment, and reluctance of vendors and users to adopt new and “disruptive” technologies.
Figure 1: A summary of the interoperability problem in public safety communications and how it might ultimately be addressed.

Now:
- Disparate, stovepiped & proprietary systems
- Segregation by choice of standard
- Rigid allocation of band & mode

Result:
Limited interoperability (e.g., Loan equipment, Crossband repeaters) **Unacceptable toll on life & property**

Barriers:
- Time required to develop standards
- Maturity of technology
- Regulatory issues (FCC)
- Cost/Time required to replace equipment
- Vendor support (risk aversion, economics)

Goal:
- Standards-based systems
- Ability to dynamically accommodate new standards
- Flexible & automatic allocation of band & mode

Result:
Intrinsically interoperable communications – systems “just work”

*A comprehensive system-based solution is probably decades away*
2.2 Network-Based Interoperability

In the mean time, the dominant paradigm for interoperability in public safety communications has involved the use of network infrastructure. This is illustrated in Figure 2(b). In this approach, separate radio networks are integrated through the use of radios that are combined “back to back” and serve as relays between disparate networks. The interconnection between the relay radios may be audio, in which case the audio received by one radio is patched to one or more other radios for retransmission. When such devices are used explicitly to achieve interoperability across different frequency bands, they are sometimes referred to as “cross-band repeaters.” Recently, internet protocol (IP) based interoperability devices have become more common [20]. In this approach, audio is digitized and distributed in the form of IP packets using standard local area network communications technology. In this case, the IP network serves the same role as the audio switch, but with much greater flexibility, including the ability to extend communications nets over long distances.

A serious limitation of network-based interoperability is poor support for uncoordinated users, as illustrated in Figure 2(c). The problem is this: To function properly, the relay radios used in the network interoperability device must be of the appropriate band & mode, and must be interconnected in a manner appropriate to the anticipated operational scenario. Thus, the users of such devices must be coordinated, meaning the bands, modes, and manner of interconnection must be known in advance of use. However, unusual circumstances may result in the need to support users which were not anticipated, and thus are “uncoordinated”. For example, a fire incident may involve local fire and police departments, whose presence would be anticipated and therefore coordinated. However, if the incident is the result of terrorism, then federal agencies and military forces might become involved, and it would be unlikely that they will have been coordinated in advance. Even if this possibility were anticipated, the additional cost involved in arranging for the use of existing network interoperability devices by these exceptional users may be prohibitive. Thus, such users will typically remain uncoordinated.

Traditionally, this problem is mitigated through the loan of radios from coordinated groups to uncoordinated users; alternatively, commercial means of communication such as cellular telephony or wireless local area networks might be employed. The former is undesirable due to the resulting delay in establishing effective communications, as well as issues with cost in maintaining additional radios for this purpose and training in the use of radios which may be unfamiliar. The use of commercial telephony is undesirable due to it’s relative lack of robustness and potential to be overwhelmed by an excess in demand during emergency situations.

It should be noted that increasingly versatile forms of network-based interoperability are becoming available. Notable is an SDR-based approach demonstrated by Vanu, Inc. [30]. This approach uses SDR to achieve a much more flexible and potentially dynamically-reconfigurable form of interoperability. The problem remains,
Figure 2: Interoperability between two disparate radio networks. (a) Two groups, using incompatible bands/modes. (b) Network-based interoperability. (c) Introducing a new uncoordinated user. (d) User-based interoperability.
however, that such a system is part of the local infrastructure, and therefore uncoordinated users could not, in the near future at least, assume that such infrastructure exists. Furthermore, to make such a system transparent to users requires elements of cognitive radio technology such as automatic signal recognition and dynamic frequency assignment, which are not yet mature and face significant regulatory hurdles.

2.3 User-Based Interoperability

Figure 2(d) illustrates an alternative to network-based interoperability: user-based interoperability. In this approach, existing and emerging heterogeneous system infrastructure continues to operate or is installed without modification, but is accessed in a seamless and transparent manner by means of a single radio. This radio is the subject of this report. Users equipped with this radio would be able to communicate in any public safety radio system, immediately and without prior coordination. Such a radio would be immediately useful to agencies at the state and federal levels, such as the FBI, which are frequently in the position of having to communicate on an emergency basis with local agencies which might be using any one of the large number of possible band/mode combinations shown in Table 1. However, such a radio would also be of great interest to local agencies as well as a means of simplifying, standardizing, and “future proofing” radio equipment.

2.4 User-Based Interoperability via SDR

A conceptual view of a radio implementing user-based interoperability is shown in Figure 3. From the user’s perspective, the radio behaves as if it contains many different radios; perhaps as many as 8 different radios assuming 1 radio per band. However, since there are frequently multiple channels of interest per band, the effective number of radios needed to achieve truly seamless interoperability is actually much greater. On the other hand, it is unlikely that the user would (or could) utilize more than just a few channels at a time. For example, the user might wish to engage in data communications simultaneously with monitoring one or more voice channels, and can only effectively engage in voice dialog on one channel at a time. Thus, this report presumes that a literal implementation of the architecture suggested by Figure 3 is not necessary, or desirable. Although recent developments in device miniaturization and integration suggest that such an approach might be possible, it would appear to be an inefficient use of hardware.

A more attractive scheme is shown in Figure 4. In this approach, a smaller number of radios are used, but each radio is an SDR with relatively wide tuning range and bandwidth spanning many channels. Each SDR is capable of tuning only one band at a time, but is capable of supporting multiple channels per band. SDR technology is particularly attractive from the perspective that the radio depicted in Figure 4 could be designed to accommodate additional/new modes through software download. This would facilitate evolving technical requirements such the bandwidth narrowing associated with transition from P25 Phase I to Phase II modes. A comprehensive
An important consideration in comparing the architectures suggested by Figures 3 and 4 is that each of the SDRs in Figure 4 is dramatically more complex than the individual radios depicted in Figure 3, especially if each SDR must support all bands shown in Table 1. For this reason, a compromise approach, incorporating aspects of both architectures, is proposed in Section 4.

SDR-enabled user-based interoperability has already been demonstrated by Vanu Corp., who have demonstrated all-software implementations of FM and P25 digital voice waveforms on an iPAQ PDA interfaced to a compact RF transceiver [32, 33]. Vanu reports that the size for their P25 waveform binary file is a modest 480 KB, takes approximately two-thirds to one second to initialize, and consumes only 24% of the available clock cycles on the PDA’s 206 MHz StrongARM processor. This is very encouraging with respect to the goal of developing a low-cost SDR-based user-based interoperability radio that offers comprehensive support for all bands and modes of interest to the public safety community.

Finally, we note that the regulatory environment has in recent years become extremely favorable for multiband/multimode SDR technology. Already, a Vanu SDR-based GSM base station has received FCC type acceptance. Thus, a radio of the type proposed here appears to be not only technically feasible, but also well within emerging regulatory bounds.
2.5 Military SDR and the SCA

The U.S. military has interoperability issues similar to those of public safety radio, and in response has been working to develop flexible radios of the type described here. Currently, this is being pursued through the Joint Tactical Radio Systems (JTRS) program [34]. Military SDR is maturing rapidly, and is now producing actual products [6]. At first glance, it might appear that new military SDRs, such as those becoming available as a result of JTRS, might be the basis for an immediate solution to the public safety radio problem. Unfortunately, military JTRS products are extraordinarily expensive [6]. A major factor in the expense has to do with demanding requirements that are unique to military uses. These include:

- Tuning range which is large and continuous, ranging from 17:1 (30–512 MHz) to as much as 1000:1 (2–2000 MHz) for some radios. Although public safety frequencies span a range of 200:1 (25–4990 MHz) – intermediate by comparison – this range contains large gaps in which tuning is unnecessary.

- Severe environmental requirements.

- Severe/complex security requirements.

- Need to support waveforms which are unique to military applications.

Ironically, it is not generally true that the performance of military SDRs is significantly better than that of conventional public safety radios, which is probably an indi-
A second aspect of military SDR that impacts suitability for public safety applications is the requirement for conformance with the JTRS Software Communications Architecture (SCA) [35]. An graphical overview of the SCA is shown in Figure 5. The SCA is intended to provide a unified framework for implementation of SDR software and a consistent method for describing and interfacing to SDR hardware. From the public safety perspective, however, SCA may be a “double-edged sword.” On one hand, it offers a logical and consistent environment in which to develop SDR applications, and encourages waveform portability. On the other hand, SCA-based SDRs are prone to sluggish initialization and mode switching, and tend to have expansive memory and power requirements. A more detailed consideration of the suitability of SCA in public safety applications is provided in [31], and our experiences with SCA in this project are reported in [3, 5, 8, 11, 16], with Phase I outcomes summarized in Section 3.3.2.

Even though considerable relaxation of requirements is possible for public safety applications, and even though this process could result in a lower-cost radio with similar capabilities, approaching this problem as a redesign of existing military SDR radios may pose significant risk to manufacturers. A complicating factor is the limited size of the public safety market and uncertain future of standards and regulatory efforts that impact SDR. A goal of the project described in this report is to address and mitigate these risks through the design of a prototype radio, so as to encourage the involvement of a broad array of manufacturers – not just those currently familiar with the technology – who might otherwise not be willing to invest in this market.
2.6 Summary

This report describes the first phase of effort in a project to develop an radio that offers comprehensive user-based interoperability for the public safety community. Specifically, the radio would be a one-for-one replacement of existing user radios with an all-band / all-mode radio as a practical that would provide immediate relief as well as being a means to transition to the goal architecture depicted on the right side of Figure 1. Desirable features of this approach include the following:

- The technology exists; this is primarily a just hard design problem. In particular, the challenge may be achieving a reasonable unit cost.

- Existing systems and network architectures continue to work without modification. The proposed radio provides a graceful transition to the goal architecture.

- Possibly simplified regulatory acceptance, at least compared to an immediate jump to a \textit{bona fide} cognitive radio solution.

- Immediate relief for first responders in a manner that does not require dramatic changes to systems or operations

However, this approach is still not without challenges. These include:

- Significant design risk

- New security issues to manage

- New operational/planning issues to manage

- Must not be dramatically more expensive than existing technology

- Reluctant vendor support; reluctance to invest in non-recurring engineering (NRE) required to develop such a radio.

- Reluctant user support; concern about disruptive effects of new technology.
3 Summary of Work to Date

This section summarizes work done in the effort to develop the radio described in the previous section. All effort has been documented in technical memoranda [3]–[16] available at the project web site [1].

3.1 Frequency Bands of Interest

Following guidance from the sponsor, acting on input from an advisory committee consisting of public safety communications professionals, it was decided at the beginning of the project to limit the frequency range of interest to bands above 50 MHz; i.e., not to include 25–50 MHz. Thus, the total frequency range of interest is from 138 MHz to 4.99 GHz. This is fortunate, as the effort required to include the 25–50 MHz band would dramatically increase the difficulty of the design, as discussed below.

3.2 Radio Frequency Design

The starting point for the RF hardware was the design from a recently completed project to build a “Matrix Channel Measurement System” (MCMS), an instrument developed for studies of multiple antenna radio systems [36, 37]. MCMS tunes continuously from 250 MHz to 6 GHz and supports 40 MHz digitized bandwidth. Although a straightforward revision to change the tuning range to cover 138 MHz to 4.99 GHz is possible, we decided that this was probably not the best course of action. There are two reasons.

The first reason is evident from an examination of the frequency coverage requirements, as shown in Figure 6. Note that the spectrum used for public safety applications is relatively concentrated into just a few, relatively narrow contiguous “chunks” of spectrum. Furthermore, note that bands above 1 GHz are mode-specific: Specifically, the spectrum around 2 GHz is exclusively commercial PCS, the spectrum around 2.4 GHz is exclusively wireless networking using the IEEE 802.11 family of protocols, and the spectrum around 4.9 GHz is similarly intended for broadband data applications. Although one could argue that in each band many different protocols could possibly be used, it is also true that technology already exists for effectively handling the multiple modes possible within a band. In the PCS band, for example, existing chipsets already support multiple protocols; e.g., CDMA and GSM in a single phone. Likewise, single chips now increasingly support IEEE 802.11b, 802.11g, and WiMAX; or GSM, GPRS, EDGE and WCDMA; over very large tuning ranges, despite the fact that these are very different protocols; for example [38, 39].

This is in contrast to the spectrum below 1 GHz. Below 1 GHz, the use of analog FM as well as the wide- and narrowband variants of the P25 digital voice protocols is not limited to any particular range of frequencies, and the potential exists for simultaneous operation of all three in close spectral proximity to each other and to
Figure 6: Public safety frequency requirements from Table 1 plotted on a frequency axis. The bottom plot is the same data plotted on a log_{10} scale.
broadband data modes, for example in the 700 MHz band. Unlike the situation above 1 GHz, public safety wireless modes below 1 GHz are not particularly band-specific and no off-the-shelf solution simultaneously addresses the problem of multiple bands with large tuning ranges.

As anticipated in Section 2.4, this suggests an architecture which is a compromise between Figures 3 and 4. In particular, we see an advantage in implementing the dual-SDR architecture shown in Figure 4 for coverage below 1 GHz, and covering the remaining bands above 1 GHz using existing band-specific chipsets.

The second reason for deviating from a literal implementation of the architecture described in Figure 4 pertains to the problem of antennas. In a nutshell, it is unrealistic to expect that all bands from 138 MHz to 4.99 GHz can be implemented using a single antenna. It may be possible to cover bands below 1 GHz using a single antenna. In fact, we investigated one commercially-available antenna, the Sti-Co “Mobile Interoperable Antenna,” that is claimed by the vendor to allow communications simultaneously on three bands: 150–174 MHz, 406–512 MHz, and 806–896 MHz [15]. As explained in our report, this antenna already has significant limitations. The design is intended for vehicular (roof) mounting and is not suitable for a handheld radio. Furthermore, it does not seem likely that the design concept could be extended to include bands above 1 GHz. On the other hand, this is perhaps not a serious problem as the antennas traditionally used to implement communications on bands above 1 GHz – e.g., stub monopoles, patches, and planar inverted-“F” antennas – are very compact and relatively convenient to implement as separate, discrete antennas.

Taking into account the chipset support issue described above, this suggests an approach in which the three bands above 1 GHz each incorporate separate antennas and chipsets, and the bands below 1 GHz share a single monopole-like antenna by use of an RF multiplexer – perhaps a triplexer – interfaced to SDRs. Proceeding along these lines, [12] describes an RF architecture for an SDR RF block that covers the 138–894 MHz range. As mentioned above, this design is a modification (simplification, actually) of the MCMS design, and is likely to be overkill from a performance perspective and more expensive than necessary. Thus, we are also looking into different approaches, including several recently developed single-chip direct conversion receivers and transmitters. Section 4 describes a strawman plan to incorporate these RF downconverters and upconverters into the overall radio design.

Finally, the issue of the exclusion of the 25–50 MHz band should be addressed. It should be noted that including this band would dramatically complicate the design of the radio. A rough measure of the difficulty of a receiver design is the fractional bandwidth over which the radio must tune.\footnote{This is due to the fact that many of the impairments that radios encounter pertain to frequency content at harmonics or products of frequencies which the radio receives, transmits, or uses as part of its design. The greater the fractional bandwidth, the more complex the problems become.} Reducing the minimum frequency from
138 MHz to 25 MHz is a five-fold increase in this ratio. In fact, the bottom (log-scale) plot in Figure 6 shows the problem from the perspective of a receiver designer: Accommodating the 25–50 MHz span introduces difficulty comparable to that of covering the entire span from 138–894 MHz. This issue directly impacts the antenna interface problem as well: It is quite unlikely that any antenna that performs satisfactorily in the 25–50 MHz band will be suitable for use at higher frequencies, thus the advantage in having a radio that covers both spans is not great.

3.3 Digital / Baseband Design

We have considered two approaches to the implementation of the digital/baseband processing. One approach is centered on the use of the Analog Devices Blackfin embedded processor running the $\mu$Clinux operating system [4], using a custom FPGA-based design as a digital IF subsystem [9]. The second approach is centered on the use of the Open Source SCA Implementation: Embedded (OSSIE), Virginia Tech’s implementation of the SCA, implemented on the Texas Instruments OMAP processor [8]. The first approach represents a somewhat traditional design approach, whereas the latter potentially leverages the advantages of the SCA, such as waveform portability.

3.3.1 Blackfin/$\mu$Clinux Approach

In this approach, digital IF processing is implemented completely on an Altera Stratix-class FPGA. The FPGA accepts 120 MSPS A/D output and outputs a swath of spectrum from the digital passband in complex baseband form at 468.75 kSPS. The FPGA firmware is custom Verilog HDL developed by our team. This is accepted by the Blackfin processor using a glueless asynchronous transfer using the Blackfin’s parallel port interface (PPI). The Blackfin runs the $\mu$Clinux operating system and the applications are developed in the C programming language. Recently, we demonstrated an FM receiver application in which the FPGA output is demodulated and delivered to a speaker via an embedded audio codec processor. The binary footprint of the application is 103 KB, and the total memory footprint of this application (including the operating system and memory which is dynamically allocated by the application) is estimated to be 42.4 MB. The total dynamic memory available to the Blackfin processor, implemented as on-board (but off-chip) SDRAM, is 64 MB. A detailed description of this design is provided in [14] and all source code and support files are available via the project web site [1].

3.3.2 OMAP/SCA Approach

In this approach, digital IF processing is implemented using the Ettus Research Universal Software Radio Peripheral (USRP), which uses an Altera Cyclone-class FPGA. The USRP’s FPGA accepts 64 MSPS A/D input and outputs a swath of spectrum from the digital passband in complex baseband form at 250 kSPS. The FPGA firmware is provided by the vendor. This FPGA output is via a USB 2.0 serial interface. As an interim step, baseband processing is not implemented on the OMAP
processor, but rather on a personal computer running the Linux operating system. Currently, we have demonstrated SCA-based FM receiver and transmitter applications which process audio through the PC’s sound card. The memory requirements of this implementation have not yet been determined. Efforts to port this application to the OMAP embedded processor are not yet complete. Additional integration of the OSSIE SCA implementation into the OpenEmbedded application development environment for the OMAP is required. Also, the OMAP implementation in use is unable to accept a sample rate greater than 25 kSPS; thus, a revision to the USRP firmware will be necessary to reduce its output sample rate. A summary of the current state of this development is provided in [16]. OSSIE and source code specific to this application are available via Virginia Tech’s version control system (access instructions provided in [16]).
4 Strawman Design

The efforts and findings reported in the previous section have lead us to some conclusions about a preferred implementation of the desired radio. A block diagram of this current “strawman” design is shown in Figure 7.

4.1 Antenna System

As discussed in Section 3.2, the design of the antenna is at least as significant a problem as the design of the radio. If the radio is to be used for receive only, then good matching between the antenna and the radio is not essential (although nevertheless important for sensitivity) and a single broadband or multiband antenna may be a reasonable option. If the radio is to transmit, however, then good matching is required in order to mitigate the reflection of transmitted power into the receive sections of the radio. As discussed in Section 3.2, it is proposed to implement the PCS, 2.4 GHz, and 4.9 GHz bands using separate signal paths, each with their own antenna. This is reasonable even for handheld radios because these antennas can be very compact and tightly integrated into the case of the radio (as are antennas used by most modern mobile phones and computers). However, antennas for the bands below 1 GHz will be too large to be implemented as other than traditional monopole-like antennas. At the same time, it is undesirable to implement more than one such antenna.

Being limited to one antenna, and nevertheless requiring a good match at all frequencies of interest, a RF multiplexer will be required. An RF multiplexer is a device which separates the bandwidth presented at one port into multiple smaller bandwidths, and is typically bidirectional with good impedance characteristics within the available bandwidth. Here, we believe that a triplexer (a 3-port multiplexer) will be sufficient. The triplexer should be tailored to the impedance characteristics of the antenna, although most commercially-available multiplexers simply assume a standard impedance.

As mentioned above, we evaluated a commercially-available antenna-triplexer combination that is presently being marketed to the public safety community [15]. We found that although the antenna-triplexer combination performs as promised on most counts, the frequency coverage is less than what is required in this project, and we have some doubts about the pattern characteristics of the antenna. In the context of this project, we believe it will be very difficult to prevent the design of the antenna/multiplexer combination from limiting the performance of the overall system. For this reason, we intend to implement the ability to bipass the triplexer, if desired, and use instead individual antennas connected directly to triplexer inputs.

4.2 Sub-GHz Front End (SGFE)

Assuming a triplexer is used below 1 GHz, a system will be required for duplexing receive and transmit as well as switching radios to triplexer input bands. This system
Figure 7: Strawman Design.
is referred to as the sub-GHz front end (SGFE) in Figure 7. A possible design of the SGFE is shown in Figure 8. RF downconverters (RFDCs) and an RF upconverter (RFUC) are connected to band-specific processing using a $3 \times 2$ and $3 \times 1$ RF switch, respectively. For each band, Figure 8 shows receive and transmit being combined using a circulator; however, combinations of switches and isolators may be desired or required instead. The path for each band includes a low-noise amplifier (LNA) in the receive path and a power amplifier (PA) in the transmit path. This allows the LNA and PA to be optimized for the frequency band, and removes the need to implement these separately in each RFDC and RFUC, which would be redundant and would require more expensive and exotic devices in order to support the full sub-GHz tuning range.

### 4.3 RFDCs and RFUC

For bands below 1 GHz, it is proposed to implement two RFDCs and one RFUC. Each would have an instantaneous bandwidth on the order of 40 MHz. This makes it possible to receive many channels simultaneously in up to two widely-separated bands. Since it is difficult to imagine a scenario requiring simultaneous transmission in two widely separated bands below 1 GHz, only 1 RFUC is proposed. The RFDCs produce real-valued A/D output corresponding to a digitized analog IF, and the RFUC does the same in reverse.
4.4 Digital IF & Baseband Processing

A DDC is a device – typically a single chip – which accepts sampled analog IF, tunes within the digital passband, and outputs a complex baseband signal with selectable bandwidth and sample rate. At the beginning of this phase of work, we were uncertain as to whether in this application it was best to implement this functionality in an FPGA (as described in 3.3.1) or using special function chips (as described in [36]). Our current preference is the latter, given the recent dramatic improvement in the capabilities and relatively low cost of these components. Currently, we are investigating the Analog Devices AD6636 DDC [40], which accepts input up to 150 MSPS, outputs up to 4 independent tuned outputs, and costs about $30 in 1k quantity – significantly less than the cost of an FPGA with sufficient resources to implement the same functionality. Comparable DUC chips are available.

As described above, bands above 1 GHz would utilize band-specific chipsets, which offer a much greater degree of integration and effectively leverages market forces which produce devices with the desired features. In all cases though, the common interface to subsequent processing would digital pre-detection IF at complex baseband. This interface would be through an FPGA, which for narrowband protocols would be primarily a routing instrument, but for wideband waveforms, such as CDMA, would be used for computation-intensive operations such as despreading.

As in the preliminary work described in 3.3, all subsequent processing, including modulation/demodulation of narrowband waveforms and symbol-rate processing of wideband waveforms, would be preferentially implemented in a software-defined manner in the embedded microprocessor. However, to the extent that is practical and cost-effective to do so, some of these functions could be off-loaded to the FPGA.

4.5 Higher-Level Functionality, including Security and Control

Without some careful attention to detail in the design of the higher-level functionality of the radio, it is possible that the powerful new capabilities could be abused, unintentionally or intentionally. Potential issues are addressed below.²

One concern is that the availability of an expanded set of frequencies and modes must not lead to a breakdown in network discipline. Specifically, authorized personnel must retain the ability to (a) constrain the capabilities of users, (b) maintain contact with users even as they access other bands and modes, and (c) override band/mode privileges as needed to maintain positive control over the network. To facilitate this, we envision a number of simple measures:

²This section is adapted from the material originally presented in the project proposal, and is repeated here in order to include it as part of the formal project documentation.
• **Preset Lock-ins & Lock-outs.** In this rudimentary scheme, the radio can be programmed with preset “lock-ins” (band/mode combinations that the radio must serve) and “lock-outs” (band/mode combinations that the radio is prohibited from serving).

• **Scan duration latency limits.** The radio can be programmed to limit the amount of time spent searching for activity on other channels, so as to prevent the possibility of a user being left unaware of communication on higher-priority modes/channels.

• **Away duration latency limits.** The radio can be programmed to limit the amount of time spent actually receiving or transmitting on lower priority channels. This precludes, for example, the possibility of a low-priority, long duration, high bandwidth data communication on an TIA902 mode from preventing a priority voice transmission on a P25 voice mode from being heard.

• **Digital recording and automatic playback of activity on alternate frequencies/modes.** For example, consider a user monitoring two voice nets simultaneously. If a transmission arrives on one channel while the user is listening to a transmission on another channel, then the radio records the unattended channel and plays it back automatically as soon as the transmission on the other channel ends. There are of course limitations to this functionality; for example, the two channels must be simultaneously within the 40 MHz instantaneous bandwidth of the radio, and the scheme fails if both channels are continuously active.

• **Commanded modification of privileges from a remote location.** This feature would exploit the ability of the radio to use existing, secure data transport mechanisms supported by 802.11 to pass instructions to radios. Just as it is possible to send encrypted e-mail between computers on the internet, it would be straightforward to include an off-the-shelf secure mechanism for remotely controlling or reprogramming radios through their ability to use an 802.11 mode.

Another concern is the need for security mechanisms to ensure that the radios cannot be intentionally or unintentionally misused, “hacked” over the air, or exploited to the detriment of public safety organizations if stolen or reverse-engineered. For a conventional single-band, single mode radio, this is not so great a concern because the amount of mischief that can be created by a single radio is limited. A single all-band, all-mode radio, however, could be exploited to create much greater havoc. A lapse in physical security, e.g., a stolen radio, could be mitigated by requiring entry of a unique pass code upon power-up. Because static pass codes can be compromised, it would be desirable to use a “rolling pass code” system in which the pass code changes periodically (e.g. daily) in some pseudo-random fashion so that future codes cannot be guessed and must be obtained from a network manager. A more sophisticated approach is to build in a “remote override” capability via the 802.11-based secure control mechanism identified above.
4.6 Other Specifications

Here we summarize other specifications of the radio that we will be developed in future phases of effort.

- Bands: Per Table 1, except for 25–50 MHz (as discussed in Section 3.1).
- Modes: Ability to support all modes expected to be used in each band. However, we intend to implement only TIA-603 (analog half-duplex narrowband FM voice) [10], the narrowband (6.25 kHz) CQPSK-based P25 digital voice mode [23], and a rudimentary (PHY-only) 802.11b waveform.
- Ability to operate on multiple channels simultaneously, as described above.
- Voice and Ethernet I/O.
- User-transparent VoIP direct to audio, with no additional terminal equipment required.
- Size, weight, and power all comparable to a laptop computer

4.7 Other Possibilities

We intend to continue to monitor developments in the wireless industry in order to be aware of useful new technology as it becomes commercially available. We anticipate a number of developments over the next few years that could potentially lead to dramatic improvements or simplifications of the radio of interest here. Of particular interest are developments in direct conversion RFICs with large tuning range, which could dramatically simplify the RFDCs and RFUCs. Other architectures which could lead to higher levels of integration and simplification have been reported recently [41, 42], and we will continue to monitor the progress of those.

It is also possible that switches and filters based on microelectromechanical systems (MEMS) technology are refined and suitable devices become commercially available. In particular, RF MEMS switches with power handling up to 5 W could be used to dramatically simplify the design of the SGFE, and might be employed to develop a reconfigurable antenna that might avoid many of the difficulties discussed above. Also, there is some possibility that antennas with improved bandwidth characteristics might become available (e.g., [43] indicates some progress in this direction), which would also simplify the antenna interfacing problem.
References


[37] MCMS project web site: http://www.ece.vt.edu/swe/mcms/.


E  Phase II Report

This appendix is a complete copy of the Phase II technical report, which documents various aspects of the project.
Chameleonic Radio
Technical Memo No. 23

Phase II Technical Report

S.W. Ellingson, S.M. Shajedul Hasan,
M. Harun, and C.R. Anderson

October 5, 2007
Phase II Technical Report

S.W. Ellingson, S.M. Shajedul Hasan, M. Harun, and C.R. Anderson
October 7, 2007

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1 Introduction

This report summarizes the efforts performed in Phase II of the project “A Low Cost All-Band All-Mode Radio for Public Safety,” performed under Grant No. 2005-IJ-CX-K018 from the National Institute of Justice of the U.S. Dept. of Justice. The overall goal of this project is to develop and demonstrate a radio which can operate in all bands and all modes relevant to public safety operations in the U.S. This project is documented via the project web site [1] which includes a recent overview presentation [2].

In Phase I of the project, we investigated the problem and developed some preliminary solutions. We reported our findings in the Phase I technical report [3]; discussion and conclusions from that report are not repeated here. In Phase II of the project, we have made some key design choices and begun a focused effort to develop the prototype radio. Accomplishments in that effort are reported here. In subsequent stages of the project, we will complete the prototype and evaluate the results.

The following technical memoranda were generated during this phase of the work, and should be considered part of this technical report:


2. “The Rise of All-Band All-Mode Radio,” S.W. Ellingson and S.M. Shajedul Hasan, Technical Memo 17, January 9, 2007 [5]. (Note: This is the original manuscript (complete with references) that eventually became a MissionCritical Communications article [6].)

3. “Blackfin-Based Continuous Baseband Processing,” J. H. Oh and S.W. Ellingson, Technical Memo 18, April 1, 2007 [7]. (Design files described in this report are available via [1].)


Achievements since the Phase I technical report include:

• Further development of Blackfin-based baseband processor software development [7].

• Developed prototype superheterodyne RF frequency converters [4].

• In collaboration with Motorola, developed an alternative architecture based on a new direct conversion radio frequency integrated circuit (RFIC) [12]. The motivation for this was documented in [5] and presented in [13]. This approach appears to have dramatic consequences for cost and possibly also size, weight, and power.
• Preliminary versions ("3b" and "4") of the Motorola RFIC, provided as an evaluation board by Motorola, have been evaluated at Virginia Tech with results that appear promising for public safety applications [8, 10]. We have subsequently designed and constructed our own prototype board [11] to begin the process of design integration using RFIC version 4, and have again confirmed the expected performance (report pending).

• Developed an “optimum noise figure specification,” addressing a problem that emerges in the design of receivers based on direct conversion architecture with very large contiguous tuning range [9].

• Evaluated the Analog Devices AD6636 digital downconverter chip, using an evaluation board of our own design. The need for this chip has diminished due to our decision to change the architecture, but it is still potentially useful as a baseband channelizer.

This report is organized as follows. Section 2 ("Architecture I") provides an update on the development of the superheterodyne-based architecture proposed in the Phase I technical report. Section 3 ("Architecture II") presents the new architecture based on the Motorola direct conversion RFIC, including some discussion of the motivation for this architecture and a summary of the design as it now stands. Section 4 ("Evaluation and Development Using the Motorola SDR RFIC") provides a brief overview of work done to evaluate the performance of the Motorola RFIC and to begin the process of design integration.
2 Architecture I

In this section we report on work on the first architecture considered for the radio, first described in [3]. We shall refer to this as “Architecture I” to distinguish it from the subsequent (current) direct-conversion architecture, reported in Section 3. The defining feature of Architecture I, as shown in Figure 1, is the use of superheterodyne block frequency converters with the analog/digital interface implemented at a VHF-band intermediate frequency (IF). For a detailed discussion on the motivation and considerations for this architecture, the reader is referred to [3]. In this section, we report on progress made on various elements of the architecture since [3]. It should be noted that Architecture I is no longer being pursued, for reasons discussed below and in Section 3.

2.1 Superheterodyne Block Frequency Converters (RFDC & RFUC)

The superheterodyne block frequency converters indicated in Figure 1 were designed, prototyped, and evaluated. The resulting hardware is shown in Figure 2. The converters tune 138–894 MHz continuously using the same frequency plan with 2 local oscillators (one tuned, one fixed). The IF is 78 MHz with an instantaneous bandwidth of 40 MHz. The gain, noise figure, and input third-order intercept point (IIP3) of the downconverter are 47 dB, 4.5 dB, and $-32$ dBm, respectively.

The downconverter layout occupies 139 cm$^2$ and consumes 280 mA at 9 VDC, however no specific attempt was made to minimize footprint or power consumption in this prototype. The parts cost of the downconverter is about $185 in small quantities; however this is estimated to increase by about 25% in a subsequent prototype in order to increase IIP3 to a more reasonable value (greater than $-10$ dBm). Design and measurement details on the downconverter are available in [4]. Details on the upconverter were never documented in the form of a report as the decision to switch to Architecture II occurred while this was underway; however these details are freely available from the authors.

2.2 Digital Downconverter (DDC)

The digital downconverter indicated in Figure 1 was designed, prototyped, and evaluated. The Analog Devices AD6636 [14] was selected for this purpose. The block diagram of the AD6636 is shown in Figure 3; the compelling feature of this chip is the ability to accept a 104 MSPS digitized IF (as would have been produced in Architecture I) and reduce it to 4 independently-tuned channels with selectable bandwidth and sample rate. In addition, the part is extremely compact (see Figure 4) and currently costs less than $30 in large quantities. The prototype hardware developed to evaluate the AD6636 is shown in Figure 4. We were able to verify baseband (bandlimiting & sample rate reduction) functionality, but were unsuccessful in implementing tuning. Work attempting to resolve the problem was underway but halted once it became clear that this part would not longer be required due to the switch to Architecture II. Details including board design and firmware are freely available by contacting the authors.

2.3 Baseband Processing

In our Phase I report [3], we described two possible implementations for baseband processing: One approach centered on the use of the Open Source Software Communications Architecture (SCA) Implementation: Embedded (OSSIE), Virginia Tech’s implementation of the SCA, implemented on the Texas Instruments “OMAP” processor; and the second approach centered on the use of the Analog Devices Blackfin embedded processor running the $\mu$Clinux operating system, with
Figure 1: Architecture I. “SGFE” stands for “sub-GHz front end.”
Figure 2: Superheterodyne block frequency converters.
Figure 3: Block diagram of the AD6636 DDC chip. From [14].

Figure 4: AD6636 DDC chip being evaluated on a custom board designed by VT for this purpose. The AD6636 is the square chip in the bottom center; top left is an FPGA and top right is a first-in first-out (FIFO) capture buffer.
processing burden divided between custom FPGA-based firmware and the C-language source implemented on the Blackfin. The latter represents a somewhat traditional design approach, whereas the former potentially leverages the advantages of the SCA, such as waveform portability. Since the release of the Phase I technical report we have encountered intractable difficulties in implementing SCA in the desired platform, and judged the time and effort required to resolve the difficulties to be prohibitive. For these reasons, we discontinued the SCA development work in Fall 2006. For additional details, the reader should contact the leader of that effort, J.H. Reed (reedjh@vt.edu). Progress on the other (FPGA+Blackfin) approach since the Phase I report is discussed in [7], and scope of the problem has been greatly reduced by the transition to Architecture II, in which signals are digitized in zero-IF/complex form thereby eliminating digital processing stages associated with tuning and bandlimiting.
3 Architecture II

In this section, we report on work on the second (and current) architecture considered for the radio. We refer to this as “Architecture II” to distinguish it from the previous (deprecated) superheterodyne-based architecture described in Section 2. The defining feature of Architecture II, as shown in Figure 5, is the use of a single direct-conversion RFIC with analog/digital interfaces implemented at baseband (i.e., zero-IF/complex form); the motivation for this approach is discussed in Section 3.1, including a description of the Motorola “SDR RFIC” employed in this project. Section 3.2 discusses the approach used to design a suitable front end for this RFIC. Additional details on the implementation shown in Figure 5 are provided in Sections 3.3–3.6.

3.1 Motivation for Direct-Conversion Architecture

Superheterodyne architecture, as represented in Architecture I, is the classical approach to multiband/multimode radio design, especially when wide bandwidths and tuning ranges are required. “Superhets” meet wide tuning range requirements using a “divide and conquer” strategy in which the tuning range is divided into smaller ranges, and each is served by different IF stages which are switched in or out as necessary. In fact, this is the principle at work in many existing products including dual-band VHF/UHF radios and multiband receive-only radios, such as scanners. However, this approach becomes prohibitively complex and expensive as the number and span of the tuning ranges increase.

The alternative, represented by Architecture II, is direct conversion. It became possible beginning in the mid-1990’s to implement nearly-complete direct conversion receivers and transmitters capable of very large tuning range on a single chip. This dramatically reduces the cost and size of a radio capable of covering a large tuning range, but leaves two problems unsolved: (1) front ends capable of providing the necessary selectivity over the new, larger tuning range, and (2) suitable
Figure 6: Motorola’s 90 nm CMOS direction conversion “SDR RFIC”. Each of the 5 receive paths and 3 transmit paths tune 100 MHz – 2.5 GHz, with 8 kHz – 10 MHz (adjustable) bandwidth. Noise figure is 4.5 dB (500 MHz). Phase noise is $<-100$ dBC/Hz @ 1 kHz (500 MHz). Sideband suppression $\sim 35$ dBc (receive) and $>35$ dBc transmit without adjustment and can be improved by 10 dB or more using programmable parameters. The layout shown is 4 mm × 5 mm.

Circuitry to correct DC offset and self-mixing problems inherent in direct conversion to the levels required to meet the stringent requirements of key market sectors, including public safety. Until recently, these issues have offset the advantages of direct conversion architecture for high performance applications. The key to solving both problems has turned out to be the implementation of direct conversion transceivers in deep submicron complementary metal-oxide-semiconductor (CMOS) technology – the same low-cost process technology commonly used to implement modern digital circuits [15]. Although process variations and the limited fidelity of CMOS device models pose considerable (and continuing) difficulties for RF chip designers, a direct conversion RF transceiver and its associated digital processing can now be implemented on a single chip, and corrections for DC offset and self-mixing can be implemented using digital functionality located in the “left over” spaces on the chip. This has led to compact RF-CMOS direct conversion transceivers that span astounding tuning ranges with performance and bandwidth sufficient for almost any wireless application in the tuning range [16].

An example of such a chip is Motorola Research Laboratory’s 90 nm CMOS “SDR RFIC,” announced in June 2007 [12]. A block diagram and summary of specifications appears in Figure 6. We have been collaborating with Motorola since January 2007 to evaluate this chip, with results discussed in Section 4.
3.2 Front End Design for Direct Conversion RFICs with Extreme Tuning Range

A major disadvantage in the direct conversion architecture in our application, from the receiver perspective, is the need for a front end which is simultaneously broadband and capable of providing the necessary selectivity. However, there are several approaches which might be considered viable. First, the RFICs themselves have reduced cost and size sufficiently that it is not unreasonable to consider employ multiple transceivers operating in parallel, each of which can be directly connected to an off-chip filter bank without switches. At a cost-size point of about US$70 and 20 mm$^2$, the Motorola SDR RFIC certainly falls in this category. However, we seek approaches in which the design might be simplified as much as possible, including minimizing the number of RFICs. RF micro-electromechanical switch (MEMS) technology is gradually emerging as a possible enabling technology: RF-MEMS provide the ability to switch the outputs of a fixed filter bank to one transceiver, or to switch reactive components within a single filter to implement tuning. Another strategy is reconfigurable matching, in which the transceiver is attached to the antenna by means of a matching section with variable and automatically-controlled impedance characteristics [17]. Variability is achieved through the use of PIN diodes or RF-MEMS devices to switch reactive components into or out of the circuit, possibly also through the use of varactors (electrically-variable capacitances). Recent work has demonstrated that relatively simple circuits can achieve surprisingly good broadband performance with potential to achieve this over large tuning ranges [18, 19]. Other approaches include direct oversampling with integrated digital filtering. Examples of the practical implementation of these concepts are now common (e.g. [20, 21]).

Unfortunately all of these front end strategies (except for the first – multiple RFIC approach) share several limitations that are quite onerous for our application. First, all are limited by the fundamental Fano limits for matching bandwidth [22] with the result that none can efficiently provide more than 10’s of kHz instantaneous bandwidth at frequencies in the VHF band when electrically-small antennas are used. Second, none address the issue that virtually all modern RFICs require differential (balanced) inputs, whereas mobile antennas such as monopoles and planar inverted-F antennas (PIFAs) are almost always single-ended (unbalanced). As a result, baluns are required between the antenna and the RFIC. Because the balun must be very compact, it is typically implemented as a surface mount transformer, which has frequency limitations which are typically a compromise with respect to tuning range requirements. For example, compact transformer-based baluns which perform well from 500 MHz to 2.4 GHz are readily available, whereas suitable devices for 500 MHz and below are either unacceptably large or are unable to cover the entire tuning range.

The approach we are taking in Architecture II could be referred to as “antenna-transceiver co-design,” with the goal to overcome some of the existing antenna and front end limitations identified above. It should be emphasized that this is distinct from the concept of “active integrated antennas” in which transceiver electronics are literally built into the antenna; e.g. as in [23]. The paradigm we currently follow is illustrated in Figure 7. In the receive case, the problem becomes one of interfacing a single antenna to the multiple direct conversion receivers on the RFIC. The interface takes the form of an RF multiplexer (e.g., a diplexer if two bands, a triplexer if three bands, and so on) which separates the antenna output into appropriate frequency ranges, thereby providing sufficient selectivity for subsequent direct conversion tuning. Although the design of RF multiplexers is an old problem, the existing literature is overwhelmingly focused on the problem of interfacing single-ended devices with roughly constant impedance (e.g., wideband antennas, or narrowband antennas over small fractional bandwidth) to other single-ended devices with roughly
constant impedance [24]. In contrast, the impedance of compact antennas operating over large fractional bandwidths varies from extremely capacitive with very high $Q$ (hence inherently narrowband) at low frequencies, to wildly variable at higher frequencies as various disparate current modes become more or less important with varying frequency. The latter is particularly frustrating as it complicates the already difficult problem of physical integration of the antenna into the radio chassis. This has only very recently begun to be considered in the context of multiplexer design [25]. Moreover (as explained above) modern transceiver RFICs require differential interfaces, whereas conventional compact antennas are either nominally single-ended or turn out to be multimoded in complex, undesirable ways.

At frequencies below first resonance of the antenna (i.e., the “electrically small” antenna case), high $Q$ makes broadband matching futile. However broadband external (“environmental”) noise plays an increasingly significant role at frequencies at which handset antennas become electrically very short; i.e., at VHF and below. External noise can easily be strong enough to become the dominant contribution to receiver noise temperature, resulting in the counterintuitive situation in which the antenna-receiver interface can be severely mismatched and yet achieve nearly optimum sensitivity because the antenna-receiver mismatch degrades signals of interest and the dominant environmental noise in equal measure. In other words, signal-to-noise ratio becomes independent of the match as long as noise figure is sufficiently low. This finding has been recently been exploited in the design of front ends for low-frequency radio telescopes to achieve noise figures limited only by the irreducible and ubiquitous Galactic synchrotron radiation background [26] over bandwidths of $> 25\%$ at VHF using antennas with relatively narrow impedance bandwidth [27]. This provided the motivation for our work on “optimum noise figure” specifications, documented in [9]. In the present problem, it is possible exploit this principle by being flexible in the quality of the match achieved and trading off the degraded efficiency for increased bandwidth, to the maximum extent

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1 Following common practice, the term “mode” in this report is used to refer to both protocol (e.g., analog FM) and electrical representation (e.g., differential). Apologies for any confusion this may cause.)
allowed by the Fano bound in combination with practical component limitations. This approach leads to specific bounds on the noise figure of the front end in order to ensure that the combined environmental and internal noise contributions remain acceptable, and leads to a complex but interesting and potentially productive co-design problem. We refer to front end circuits designed according to these criteria as being “environmental noise-limited optimization” (ENLO) stages.

The observation that radios can have external noise-limited sensitivity is hardly new, but neither is it broadly appreciated or fully exploited. The principle is most commonly mentioned with respect to “active antennas” of the current- and voltage-sensing types described in classic references by Rhode [28], Nordholt [29], and others. However, the application is quite general and presently, due to advances in amplifier components, rather broadly applicable.

Referring to Figure 7, note that it is entirely possible for the active gain stage(s) of an ENLO front end to be located at the output of the multiplexer, as opposed to serving as the multiplexer input interface. This offers the opportunity to tailor the gain stages to frequency bands, as well as providing a measure of relief from strong out-of-band signals through preselection. However in this case one can also exploit the ENLO condition to relax multiplexer channel design requirements. For example, the insertion loss can be dramatically increased, with no penalty to sensitivity as long as the external noise-limited condition is maintained. This can be directly traded-off for an increase in bandwidth, in accordance with the relevant Fano (reflection coefficient vs. bandwidth) constraint. The increased insertion loss in turn reduces the likelihood of interaction with other multiplexer channels, simplifying the design especially in the case of multiplexers with closely-spaced channels having large fractional bandwidth – as is likely to be the case in designs with wide tuning range – where interactions between channels often turn out to be a formidable design challenge [24].

Whereas the basic active ENLO front end approach is well suited to the VHF bands, more traditional strategies are required at higher frequencies where the environmental noise floor (both natural and anthropogenic) are lower.

### 3.3 RF Receive Path

The receive path implementation is based on the strategy described in the previous section. For bands below 1 GHz, the receive path to the RFIC begins at a short whip antenna of a type traditionally used in mobile transceivers. The antenna is connected to an impedance-matched RF multiplexer stage designed according to ENLO principles, which divides the signal into four bands: 138–174 MHz, 220–222 MHz, 406–512 MHz, and 764–862 MHz. The multiplexer is shared between receive and transmit paths by means of an RF switch. Continuing on the receive path, the signal passes through an additional band-specific stage of gain and filtering before arriving at the RFIC.

Cellular, 2.4 GHz, and 4.9 GHz communications are handled separately. 4.9 GHz is received using a separate antenna, which is again shared with a transmit path using a switch. A separate dedicated 4.9 GHz downconverter is used provide an intermediate frequency (IF) signal at a frequency which the RFIC can accept. Cellular and 2.4 GHz are handled using dedicated antennas and commercial chipsets, and the RFIC is not used at all. This decision is based on the common availability of these chipsets and relative ease with which efficient external antennas suitable for these bands can be integrated into the radio.
3.4 RF Transmit Path

The RFIC directly creates three outputs: one for VHF (138–174 MHz and 220–222 MHz), one for UHF (406–512 MHz and 764–862 MHz), and an IF for subsequent upconversion to 4.9 GHz. The VHF and UHF paths include parallel independent power amplifier stages, whose outputs are interfaced to the antenna through the same impedance-matched multiplexer used for the receive path. The connection between receive and transmit paths is through switches; thus operation in the VHF, UHF, and 4.9 GHz bands will be strictly half-duplex. As in the receive path, Cellular and 2.4 GHz communications are handled separately using dedicated antennas and commercial chipsets, and the RFIC is not used at all.

3.5 ADC and DAC

In Architecture II, analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) operate at baseband, sampling the low-pass I and Q signals in the first Nyquist zone. Here we have tentatively selected the Analog Devices AD9248 [30] and AD9761 [31] devices as our ADC and DAC respectively. The AD9248 is a dual 14-bit ADC sampling 20 MSPS (in the variant we have selected) which consumes about 65 mA at 3V. This allows digitization of signals up to about 10 MHz bandwidth with modest anti-aliasing requirements. The AD9761 is a dual 10-bit interpolating DAC which we operate a 20 MSPS and which consumes about 50 mA at 3V. A compelling feature of this part is the availability of internal 2\times interpolation filters which lead to a significantly reduced requirement for anti-alias filtering. A prototype ADC/DAC board including both the ADC and DAC has been designed and is currently under construction.

3.6 Baseband Processing

In Architecture I we proposed a combination of an FPGA and an Analog Devices Blackfin microprocessor for baseband processing, with the former facilitating tedious high-rate processing tasks and the latter handling low-rate processing tasks as well as audio I/O, user interfaces, and so on. While this still seems to be a reasonable choice, we are impressed with the latest generation of FPGA-based “system on a programmable chip” (SOPC) functionality and in particular the latest generation of FPGA-based configurable soft-core processors. In this approach, the functionality of the microprocessor in the previous arrangement is implemented in the FPGA. Although this could be done to some extent without employing a soft-core processor, the advantage of this approach is that the FPGA literally becomes a microprocessor, providing the associated benefits including programmability in high-level languages (in particular, C) and straightforward interfacing to peripheral devices. Additional advantages are that (1) a soft-core processor implemented on an FPGA can be tailored to requirements, i.e., functionality which is not required does not need to be implemented, (2) unfettered access to FPGA resources not used by the soft-core processor are preserved, and (3) the inevitably awkward interface between FPGA and microprocessor is eliminated, since both reside on the same chip.

We believe that some combination of SOPC and soft-core processor technology implemented in a single FPGA may turn out to be a better overall choice in terms of space, power, and cost than separate, dedicated FPGA and microprocessor chips. Both of the leading manufacturers of FPGAs – Altera and Xilinx – now provide this capability. We are inclined to use Altera devices, for which the associated capability is known as “SOPC Builder” for SOPC design and “Nios II” for configurable soft-core processor design [32]. We are currently targeting the Altera “Cyclone III” family of FPGAs.
4 Evaluation and Development Using the Motorola SDR RFIC

In this section we elaborate on our efforts to evaluate the Motorola SDR RFIC and to begin the process of integration into our design. For an overview of the chip, see Section 3.1 of this report. Our evaluation efforts began with lab testing at Virginia Tech of evaluation boards provided by Motorola. We tested two boards: one using “Version 3b” of the chip, and one using “Version 4” of the chip (shown in Figure 8), with results documented in [8] and [10], respectively. Some key results are summarized in Table 1.

Version 4 of the chip has some issues that will require considerable attention in the final design. Chief among these is that the chip requires significant calibration and “tweaking” in order to perform to an acceptable level in each band used. This involves manipulation of a large number of parameters stored in parameter registers on the chip, accessed via a low-bandwidth SPI connection. It is not currently known how often calibration will be required to maintain an acceptable level of performance, and to what degree parameters will need to be varied as the chip is tuned across various frequencies or as other parameters are varied. An important parameter affected by this issue is receive sideband rejection. Another potential issue is that the transmitter output exhibits intermittent out-of-band spurs (e.g., on the order of −60 dBc with 10 MHz spacing) that are impossible to suppress through filtering in the front end envisioned for Architecture II, since it relies on the RFIC for selectivity within a multiplexer channel. The extent to which these spurs...
<table>
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<tr>
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<td>Rx Noise Figure</td>
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<td>20 to 40 dB w/o optimization</td>
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<td>&lt; −123 dBc/Hz @ 25 kHz</td>
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</table>

Notes:
(1) The main obstacle to realizing this tuning range is the off-chip balun (if used); no commercially available balun covers the entire tuning range.
(2) Optimization requires calibration and adjustment of parameters via an SPI port. Significant improvements possible; indicated results obtained with relatively little effort.
(3) Chip consumes approx. 40 mA for receive, 40–90 mA for transmit, and 80 mA per active DDS. Current drain never observed to exceed 400 mA. Evaluation board operated at 280 mA @ 10V.

Table 1: Summary of RFIC testing.
might be reduced in future versions of the RFIC or reduced by adjusting parameters is currently unknown.

As a step in developing a complete radio using the chip, we have developed our own evaluation board using Version 4 of the RFIC; this design is documented in [11] and shown in Figure 9. This board operates as expected and a report on its performance is currently being written.
Acknowledgments

The authors are thankful to Neiyer Correal, Bob Stengel, and Gio Cafaro of Motorola for providing RFIC chips and evaluation boards, as well as extensive and patient technical assistance.
References


[6] S.W. Ellingson and S.M. Shajedul Hasan, “What’s in Radio’s Future? All-band all-mode radio could solve interoperability challenges,” MissionCritical Communications, March 2007, pp. 50-60. (Note: The published version was heavily edited, including changing the title and (unforgivable!) removing the references! The complete version including the references is [5].)


F Phase III/IV Report

This appendix is a complete copy of Technical Memo 26 (a paper presented at *Software Defined Radio (SDR) ’08*, Washington DC, October 2008) which summarizes efforts during Phases III and IV of the project.
MULTIBAND PUBLIC SAFETY RADIO USING A MULTIBAND RFIC WITH AN RF MULTIPLEXER-BASED ANTENNA INTERFACE

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ABSTRACT

Various public safety personnel often cannot readily communicate with one another due to the lack of interoperability in their radios. One of the solutions to this problem is to provide user a multi-band multi-mode radio (MMR). In this paper we present the design of an experimental prototype multiband radio, which operates in public safety frequency bands from 100 MHz to 1 GHz. In our design we use a direct conversion CMOS transceiver RFIC developed by Motorola Research Laboratories, which covers the frequency range 100 MHz to 2.5 GHz and contains multiple receivers and transmitters. Although direct conversion has some significant advantages over superhet-based design particularly due to its low power consumption and cost, there is a significant challenge to achieve performance comparable to existing single and dual-band radios. Furthermore, it is difficult to cover all of these bands using the same type of monopole antennas already in common use. Our design employs a multiband antenna-transceiver interface consisting of an RF multiplexer which yields acceptable overall performance for operation in public safety frequency bands using a simple monopole antenna. An FPGA is used to implement all the digital signal processing and a small Gumstix computer including a touch screen LCD is used as a user interface.

1. INTRODUCTION

Multiband multimode radio (MMR) is a class of radio which can operate in multiple frequency bands using multiple modes. This is a desirable solution to solve interoperability problem in public safety applications [1, 2]. In this paper we present an experimental prototype design for a low-cost MMR which provides simultaneously very large instantaneous bandwidth (up to 10’s of MHz) to process multiple channels concurrently and very large tuning ranges to cover multiple bands of frequencies. This paper follows up on our previous paper [3], which described our motivation and early stages of development. Figure 1 shows the image of our designed prototype. Detailed description and all the documents related to this are available at the project website in [4].

2. HIGH LEVEL SYSTEM DESIGN

This paper is organized as follows. Section 2 describes the high level system design, whereas Section 3 presents the description of the RFIC, which we used to design this MMR. Description of the novel RF front end is presented in Section 4. Section 5 briefly discusses the digital signal processing and a more detailed description of the prototype is given in Section 6.
are connected with the two transmit ports of the RFIC.

RFIC receiver channels convert the incoming RF signal to baseband differential in-phase (I) and quadrature-phase (Q) analog signals. A/D converters digitize these I and Q signals and send these to an FPGA for further processing. In transmit, the D/A converters convert digital transmit signal from FPGA to analog I and Q signals and send these to the RFIC, which upconverts to the carrier frequency by direct conversion. All the modulation/demodulation and digital signal processing are implemented in the FPGA. We also designed an audio board which interfaces a conventional handheld PTT speaker/microphone to the FPGA via a separate CODEC. A compact Gumstix computer including a touch screen LCD are used as a user interface of this radio [5].

3. MULTIBAND DIRECT CONVERSION RFIC

Although superheterodyne architecture has been preferred for public safety MMR for many years, the design gets complicated, expensive and power hungry if we want to cover large range of frequencies using this approach [2]. Direct conversion can be an alternative approach that alleviates these problems, but historically has been shunned due to limited performance. Motorola Research Laboratories has recently developed a multiband direct conversion RFIC using 90 nm CMOS [6]. Figure 3 shows the internal block diagram of this prototype RFIC. This IC is designed for the operation in 100 MHz to 2.5 GHz frequencies. Three independent direct digital synthesizers (DDS) are used to provide local oscillator (LO) signals to the receivers, transmitters, and feedback signal sources from a common 1GHz PLL. The only external reference signal required is 31.25 MHz at -10 dBm.

Figure 3: Internal block diagram of RFIC.

There are five receiver paths which share a common analog baseband low pass filter section with programmable corner frequency in approximately 10% steps from 4.5 kHz to 10 MHz. There are provisions for DC offset correction and dynamic matching [7]. These result in significant improvements in IP2, LO flicker noise, and DC offset compared to previous RFIC-based direct conversion designs.
Similarly, there are three transmitters which share a common baseband input. Differential baseband in-phase and quadrature-phase inputs from external digital-to-analog converters (DACs) are applied to programmable low pass filters similar to those of the receiver with 10% bandwidth steps from 6 kHz to 10 MHz bandwidth. There are three selectable transmitter paths with up to 75 dB (30 dB continuous and 45 dB stepped power control) of on chip programmable gain available (power control). A transmitter feedback network is provided for closed-loop narrow band linearization or open-loop alternative transmit signal analysis and processing.

The RFIC is configured and controlled using a serial peripheral interface (SPI) link. Approximately 262 registers are programmed to set the various parameters.

Prior to using this RFIC in our design, we evaluated it using several standalone evaluation boards and found performance to be generally consistent with specifications published by Motorola [8, 9].

Figure 4 shows the implementation of the RFIC in the current MMR prototype. Since the receivers in the RFIC require differential signals, transformers have been used as a baluns to convert between single-ended to differential signals. Ports Rx-1 to Rx-4 use the M/A-COM ETC1-1-13 1:1 transformer (frequency range 4.5 to 3000 MHz). Similar to the receiver section, the RFIC also provides the transmitter output in differential form, which is converted into single-ended using a transformer. Tx-1 and Tx-2 ports use the M/A-COM ETC4-1T-7 1:4 transformer (frequency range 6 to 1000 MHz).

Without optimization, the measured average gain of the receiver section of RFIC is 48 dB, input 1dB compression point is -26 dBm and the sideband rejection is around 29 dB. Average transmitter output power is -4 dBm, output 1dB compression point is -5 dBm and average sideband rejection is 22 dB. The performance of this RFIC, specifically the sideband rejection, can be improved significantly if we optimize the various programmable parameters. But we have not yet attempted to do so in the current design.

During receive our current RFIC board consumes 1.1W power (10V@0.11A) and during transmission it consumes 1.7W (10V@0.17A) power.

4. RF FRONT END

New generation single-chip CMOS direct conversion transceivers create the opportunity to design a low-cost efficient multiband multimode radio. However the inherent antenna problem remains essentially unsolved for such radios; specifically how they can be integrated into the design without degrading performance or leading to objectionable sizes or shapes. To be accepted by users, these radios must achieve performance comparable to existing single- and dual-band radios, using the same type of monopole antennas already in common use.

Figure 5 shows the front end/antenna interface concept using multiplexer. Our front end/antenna interface concept is shown in Figure 5. Taking advantage of the Motorola RFIC’s parallel transceiver architecture, we designed a four channel RF multiplexer, one side of which is matched with the antenna impedance and the other side is matched with the impedance of RFIC input/output ports. This design is documented in detail in [10], and the board-level implementation is shown in Figure 6. This front end board contains RF multiplexer filters as well as amplifiers, additional bandpass filters and variable attenuators to control receive gain. This front end has acceptable overall performance for operation in four bands – 138–174 MHz, 220–222 MHz, 406–512 MHz, and 764-862 MHz – when used with a monopole just 20 cm long with 5 mm radius. This is achieved not from an impedance-
matching perspective, but rather from the perspective of receive sensitivity. Specifically, we have designed the multiplexer in such a way that the receiver is guaranteed to have sensitivity which is external-noise dominated if the receive noise figure (determined by electronics following the multiplexer) can be constrained to be no worse than 1-2 dB. Although our existing design does not currently achieve this, such a noise figure is within the capabilities of existing low-cost electronics.

Figure 7 shows the circuit topology used in each multiplexer channel. Performance of our designed multiplexer is presented in Figure 8. These results are expressed in terms of transducer power gain (TPG), defined as the ratio of power delivered by a matching network to a load, to the power delivered to a perfectly matched load directly from the antenna. Although the performance in 138-174 MHz appears to be poor, the resulting sensitivity turns out to be limited only by environmental noise under the conditions described above. Furthermore, the intentionally degraded efficiency of the 138-174 MHz channel enables improved efficiency in the other bands, as we explained in the next paragraph. For transmit operation, this filter would be switched to a more conventional match for improved efficiency.

The front end design procedure is as follows. Our design criteria to achieve the maximum possible sensitivity are that the ratio of external (unavoidable) noise to internally generated noise at the output of a receiver front end should be large, and the TPG should be reasonably flat over the passband. We started our design using fifth order Chebyshev bandpass filters and performed joint optimization changing the component values to achieve maximum flatness for the first two channels and to get the maximum TPG for the other two channels.

5. DIGITAL SIGNAL PROCESSING

The differential I and Q signals from the RFIC is digitized using the AD9248 dual 14-bit A/D converter from Analog Devices. Similarly, the AD9761 dual 10-bit D/A converter is used to provide differential analog I and Q signals. Figure 9 shows the image of the ADC/DAC board. All of our digital signal processing is performed in an Altera Stratix II FPGA. This FPGA is extreme overfill for this application; only about 5% of the logic elements are used for single channel analog FM. This FPGA was chosen to facilitate experimentation with multiple simultaneous modes at a later time. The firmware is written completely in Verilog HDL.
We used EP2S60 Stratix II DSP development board from Altera for convenience in implementation, as it includes also a suitable CODEC. This board communicates with the ADC/DAC board through an 80 pin ADI connector.

6. CURRENT STATUS OF THE PROTOTYPE

Our experimental prototype multiband multimode radio is able to operate in 138–174 MHz, 220–222 MHz, 406–512 MHz, and 764-862 MHz public frequency bands. Reception and transmission of narrowband FM signals have been demonstrated in all of the above frequency bands. A separate audio daughter board which contains push-to-talk circuitry, microphone and speaker amplifiers, has been implemented to send the PTT signal to FPGA. The whole radio is controlled using a Gumstix computer through a touch screen LCD panel. When the user selects a frequency from the touch screen LCD, the Gumstix programs the RFIC through SPI and sends the channel information to FPGA for controlling the Rx/Tx switches and attenuation in the RF front end board. The Gumstix computer is used just as a user interface and no digital signal processing is implemented in it.

This prototype consumes approximately 1.5A of current at 16V. We use a 4A.hr battery to operate the whole radio, which lasts for about 1.5 hours at this current draw. No attempt has been made to optimize power consumption. Although we implemented just narrow-band FM in our current design, it is possible to implement more modes in FPGA without any change in the hardware configuration, as explained above.

A goal of this work has been to determine whether the new direct conversion RFICs can replace existing superhet architectures. We have found there some issues (specifically image rejection and selectivity) which remain to be improved to implement this in an actual product. Much work in optimization of programmable parameters in the RFIC remains. In order to get the full benefit of differential design the RF front end including the RF multiplexer filters should be transformed into differential from single ended topology. A good user interface is also necessary.

7. ACKNOWLEDGEMENTS

This project is supported by the National Institute of Justice of the U.S. Dept. of Justice under Grant No. 2005-IJ-CX-K018. The authors are thankful to Gio Cafaro, Bob Stengel and Neiyer Correal of Motorola Research Laboratories for providing RFIC chips as well as extensive and patient technical assistance. Also thanks to Rithirong Thandee, Mahmud Harun, Kyehun Lee and Philip Balister for their assistance during this project.

10. REFERENCES

G RF Multiplexer Design Paper

This appendix is a complete copy of Technical Memo 25 (a paper presented at the *IEEE Int'l Antennas & Propagation Symp.*, San Diego, CA, July 10, 2008), which describes our approach to antenna-receiver integration using an RF multiplexer. See the project web site for the associated presentation slides.
Multiband Antenna–Receiver Integration using an RF Multiplexer with Sensitivity-Constrained Design

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1 Introduction

Mobile and portable radio is an essential component of commercial, military, and public safety operations, with systems in many frequency bands ranging from HF through SHF. This profusion of frequencies and associated modes complicates interoperability and, especially in the case of military and public safety applications, significantly impacts operational effectiveness. Inexpensive high-performance multiband radios may be part of the solution to this problem. Such radios are on the verge of becoming possible as a result of emerging single-chip transceiver technology [1,2]. An aspect of this problem which remains essentially unsolved is how suitable antennas can be integrated into the design without degrading performance or leading to objectionable sizes or shapes. To be accepted by users, these radios must achieve performance comparable to existing radios, using the same monopole-type antennas already in common use. Developing antennas which perform well over many bands each representing large fractional bandwidths is a daunting task, especially at VHF and below where resonant-mode operation is typically not possible. Thus, any impedance match between antenna and receiver which achieves efficient power transfer will necessarily have unacceptably narrow bandwidth [3], and therefore will need to be tuned as the channel changes. Such a scheme is difficult to implement in trunked or otherwise frequency-agile systems, and furthermore precludes the possibility of simultaneous multi-frequency reception which is of interest especially in cognitive radio applications.

In this paper we consider an alternative approach which exploits the fact that the single-chip transceivers from which practical multiband radios are likely to be built (e.g., [2]) consist of multiple receivers operating in parallel, each of which can be directly connected to a dedicated off-chip filter. In this case an RF multiplexer can be used to segment the tuning range into multiple bands. Once partitioned in this manner, the interface for lower frequency bands – the most troublesome as noted above – can be separately optimized not for match efficiency, but rather for effective sensitivity, exploiting the high levels of environmental noise known to exist at these frequencies [4]. We demonstrate the technique by designing an antenna interface which yields acceptable performance for operation in four bands – 138–174 MHz, 220–222 MHz, 406–512 MHz, and 764–862 MHz – when used with a monopole just 20 cm long with 5 mm radius, assuming front end noise figure in the range 1–2 dB. Such noise figures are well within the capabilities of existing low-cost electronics.
2 Antenna-Receiver Interface Design

The monopole is modeled as a voltage source in series with an impedance \( Z_{\text{ant}} \), which is equal to one-half the impedance a dipole (obtained using image theory) in free space. We obtain a circuit model for \( Z_{\text{ant}} \) using the method described in [5]. The circuit model and associated impedance are shown in Figure 1. We wish to interface this antenna to separate receiver inputs using the multiplexer architecture shown in Figure 2. We initially design the multiplexer channels for constant 50\( \Omega \) frequency-independent input and output impedances, neglecting the possibility of interaction, with results as shown in Table 1 and Figure 3. These results are expressed in terms of transducer power gain (TPG), defined as the ratio of power delivered by a matching network to a load, to the power delivered to a perfectly matched load directly from the antenna. Note that the performance is unacceptable, especially in the 138–174 MHz band. However, the relevant question for receive system performance is not match efficiency but rather sensitivity. Furthermore, it is well-known that external VHF-band radio noise due to natural and man-made sources can be strong enough to constrain the sensitivity of well-designed receivers [6]. Thus, we propose that the relevant design criteria are actually (1) that the ratio \( \gamma \) of external (unavoidable) noise to internally generated noise at the output of a receiver front end should be large, and (2) the TPG should be reasonably flat over the passband. The quantity \( \gamma \) is given by \( \eta(1 - |\Gamma|^2)T_{\text{ext}}/T_{\text{FE}} \) where \( \eta \) is antenna efficiency (~1 in the frequency band of interest), \( T_{\text{ext}} \) is external noise temperature (7660 K to 3760 K in areas classified as “residential” [4]), \( \Gamma \) is reflection coefficient, and \( T_{\text{FE}} \) is the noise temperature of the front end. To exploit this observation, we used the GENESYS tool of the Advanced Design System (ADS) to jointly optimize the component values of the 138–174 MHz and 220–222 MHz channels to achieve maximum flatness (thereby satisfying the second criterion), ignoring TPG. The other two channels were optimized for maximum TPG simply by tuning the value of first series inductor in each channel. The result is shown in Figure 4, with optimized component values given in Table 1. Figure 5 shows that this design achieves large \( \gamma \) in the first two channels, despite poor TPG, for front end noise figures (corresponding to \( T_{\text{FE}} \)) as high as 2.0 dB.

It should be noted that the results in Figure 5 are obtained assuming \( T_{\text{ext}} \) classified as “residential” in [9]. However, the noise associated with environments classified as “rural” are only a factor of ~3 less than than this; furthermore, one would expect the risk of intermodulation would also be correspondingly less. This suggests the possibility of a dynamically-varying optimal tradeoff between linearity and sensitivity parameterized in terms of \( T_{\text{ext}} \), which could be measured by the receiver.

References


Figure 1: Circuit model and impedance for a 20 cm monopole of 5 mm radius.

![Circuit model and impedance](image1)

Figure 2: Interface concept; each multiplexer channel uses topology shown on right.

![Interface concept](image2)

<table>
<thead>
<tr>
<th>Component</th>
<th>Channel–1 Before</th>
<th>Channel–1 After</th>
<th>Channel–2 Before</th>
<th>Channel–2 After</th>
<th>Channel–3 Before</th>
<th>Channel–3 After</th>
<th>Channel–4 Before</th>
<th>Channel–4 After</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1 (nH)</td>
<td>377.1</td>
<td>290.6</td>
<td>1357.4</td>
<td>1322.5</td>
<td>111.2</td>
<td>82.5</td>
<td>114.9</td>
<td>81.1</td>
</tr>
<tr>
<td>C1 (pF)</td>
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<td>6.9</td>
<td>0.4</td>
<td>0.4</td>
<td>1.1</td>
<td>1.1</td>
<td>0.3</td>
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<td>3.1</td>
<td>3.1</td>
<td>0.9</td>
<td>0.9</td>
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<td>C2 (pF)</td>
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<td>39.0</td>
<td>42.8</td>
<td>42.8</td>
</tr>
<tr>
<td>L3 (nH)</td>
<td>561.6</td>
<td>402.9</td>
<td>2021.9</td>
<td>2101.2</td>
<td>173.4</td>
<td>173.4</td>
<td>182.0</td>
<td>182.0</td>
</tr>
<tr>
<td>C3 (pF)</td>
<td>1.9</td>
<td>2.6</td>
<td>0.3</td>
<td>0.3</td>
<td>0.7</td>
<td>0.7</td>
<td>0.2</td>
<td>0.2</td>
</tr>
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<td>L4 (nH)</td>
<td>9.7</td>
<td>8.3</td>
<td>1.3</td>
<td>1.2</td>
<td>3.1</td>
<td>3.1</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>C4 (pF)</td>
<td>108.7</td>
<td>125.1</td>
<td>391.4</td>
<td>437.5</td>
<td>39.0</td>
<td>39.0</td>
<td>42.8</td>
<td>42.8</td>
</tr>
<tr>
<td>L5 (nH)</td>
<td>377.1</td>
<td>207.2</td>
<td>1357.4</td>
<td>1301.4</td>
<td>112.2</td>
<td>112.2</td>
<td>114.9</td>
<td>114.9</td>
</tr>
<tr>
<td>C5 (pF)</td>
<td>2.8</td>
<td>5.1</td>
<td>0.4</td>
<td>0.4</td>
<td>1.1</td>
<td>1.1</td>
<td>0.3</td>
<td>0.3</td>
</tr>
</tbody>
</table>

Table 1: Component values of the multiplexer before and after the optimization.
Figure 3: Performance of initial multiplexer assuming constant 50Ω termination impedances (solid line) and assuming actual antenna input (dotted line).

Figure 4: Same as Figure 3 assuming antenna input, after optimization (see text).

Figure 5: Ratio ($\gamma$) of environmental to front end noise in the first two channels assuming indicated front end noise figure and “residential” noise per [4].
H Design Details

This appendix includes the complete contents of Technical Memos 28–31, which together document the latest design of the radio developed in this project. These memos are presented in the following order:


See Appendix F for a high-level overview that may be helpful in interpreting the above documents.
Design and Development of an RF Front End Board for NIJ Public Safety Radio

S.M. Shajedul Hasan* and S.W. Ellingson

July 22, 2008

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1 Introduction

An experimental multi-band/multi-mode radio for public safety applications is being developed in Virginia Tech under a project sponsored by the U.S. Department of Justice [1]. The goal of this project is to develop and demonstrate a single radio which can operate in all the public safety frequency bands presented in [2, 3]. To provide context, Figure 1 shows a conceptual “board-level” overview of a prototype of the proposed radio, consisting of a RF front end board, RFIC transceiver board, ADC/DAC board, baseband processing board, and other control boards. The design and development of the RF front end (RFFE) board is described here.

Figure 1: Conceptual board-level overview.

This report is organized as follows. Section 2 presents the summary of the input/output ports of RFFE board. Section 3 describes the signal path planning and Section 4 presents multiplexer design methodology. Section 5 and 6 presents the circuit description of the amplifier and attenuator respectively. Section 6 describes the various jumper and switch settings. Section 7 concludes the report presenting the total cost. Finally, three appendices present the bill of materials, complete schematic and layout images.

2 RFFE Board Overview

Figure 3 and Table 1 present all the input/output ports of the RFFE board.
Figure 2: Image of RF Front End board.

Figure 3: Summary of RFFE board.
<table>
<thead>
<tr>
<th>Function</th>
<th>Port Name</th>
<th>Conn. Name</th>
<th>Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Receive Ports</td>
<td>RX-1</td>
<td>J6</td>
<td>RF Mux Ch-1 receive port</td>
</tr>
<tr>
<td></td>
<td>RX-2</td>
<td>J7</td>
<td>RF Mux Ch-2 receive port</td>
</tr>
<tr>
<td></td>
<td>RX-3</td>
<td>J8</td>
<td>RF Mux Ch-3 receive port</td>
</tr>
<tr>
<td></td>
<td>RX-4</td>
<td>J9</td>
<td>RF Mux Ch-4 receive port</td>
</tr>
<tr>
<td>Transmit Ports</td>
<td>TX-1</td>
<td>J2</td>
<td>RF Mux Ch-1 or Ch-2 transmit port</td>
</tr>
<tr>
<td></td>
<td>TX-2</td>
<td>J3</td>
<td>RF Mux Ch-3 or Ch-4 transmit port</td>
</tr>
<tr>
<td>Attenuator Control</td>
<td>ATT_CTL</td>
<td>J5</td>
<td>Attenuator control signals</td>
</tr>
<tr>
<td>Rx/Tx switch</td>
<td>SW_CTL</td>
<td>J4</td>
<td>Rx/Tx switch control signals</td>
</tr>
</tbody>
</table>

Table 1: Input/Output ports of the RFFE board.

3 Analog Signal Path Planning

This section describes some considerations in planning of the RFFE analog signal path. “Analog signal path” is defined here as the section beginning at the antenna terminals and ending at the input to the analog-to-digital converter (ADC). The analog signal path under consideration contains all the circuitry in the RFFE board, which includes multiplexer, amplifier, additional filtering and attenuators, and the RFIC transceiver board described in [4].

This signal path requirements are developed following the general strategy described in [5]. In order to receive the signal and digitize it appropriately the level of incoming signal should meet the specification of ADC. In this document we use the specifications of Analog Devices AD9248 ADC described in [6]. The relevant parameters and design constraints are shown in Table 2. Given this information, we can compute the required number of bits:

$$N_b \geq 1.67 \log_{10} \frac{P_t \gamma_r}{P_{ext} \delta_r}$$

where $P_t$ is the sum of the total receive signal power plus $P_{ext}$, which is approximately equal to the total external noise power calculated using the table from [7]. Also, the minimum required gain in the analog signal path $G_{min}$, and the maximum allowed gain $G_r$ can be found using the following equations:

$$G_{min} = \frac{P_Q \gamma_q}{P_{ext}}$$

$$G_r = \frac{P_{clip} \delta_r}{P_t}$$

A summary of the analysis is provided in Table 3, which shows the values of various design parameters ($N_b, G_{min}, G_r$) corresponding to our frequency bands. Table 4, 5, 6, and 7 present the GNI analysis of the analog section for various channels using nominal gain.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{clip}$</td>
<td>+4 dBm</td>
<td>ADC full scale</td>
</tr>
<tr>
<td>$P_Q$</td>
<td>-62 dBm</td>
<td>ADC quantization noise power, referenced to ADC input</td>
</tr>
<tr>
<td>$\gamma_q$</td>
<td>+10 dB</td>
<td>Desired ratio of $P_{ext}$ to $P_Q$</td>
</tr>
<tr>
<td>$\delta_r$</td>
<td>-10 dB</td>
<td>Maximum acceptable input power relative to $P_{clip}$</td>
</tr>
</tbody>
</table>

Table 2: Assumed analog-to-digital converter (ADC) specifications and associated design constraints.

<table>
<thead>
<tr>
<th>Frequency</th>
<th>$P_t$</th>
<th>$P_{ext}$</th>
<th>$N_b$</th>
<th>$G_{min}$</th>
<th>$G_r$</th>
</tr>
</thead>
<tbody>
<tr>
<td>138-174 MHz</td>
<td>-90.0 dBm</td>
<td>-122.5 dBm</td>
<td>8.8</td>
<td>70.5 dB</td>
<td>84.0 dB</td>
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<tr>
<td>220-222 MHz</td>
<td>-90.0 dBm</td>
<td>-128.1 dBm</td>
<td>9.7</td>
<td>76.1 dB</td>
<td>84.0 dB</td>
</tr>
<tr>
<td>406-512 MHz</td>
<td>-90.0 dBm</td>
<td>-135.3 dBm</td>
<td>10.9</td>
<td>83.3 dB</td>
<td>84.0 dB</td>
</tr>
<tr>
<td>764-862 MHz</td>
<td>-90.0 dBm</td>
<td>-142.9 dBm</td>
<td>12.2</td>
<td>90.9 dB</td>
<td>84.0 dB</td>
</tr>
</tbody>
</table>

Table 3: Design implications ($N_b, G_{min}, G_r$) corresponding to various choices of frequency range and response. Gain here defined is defined from antenna terminals to ADC input.

<table>
<thead>
<tr>
<th>Section</th>
<th>Gain (dB)</th>
<th>IP3 (dBm)</th>
<th>Noise Figure (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiplexer</td>
<td>-8</td>
<td>200</td>
<td>8</td>
</tr>
<tr>
<td>Preamp</td>
<td>25</td>
<td>12.9</td>
<td>2.7</td>
</tr>
<tr>
<td>Filter</td>
<td>-1</td>
<td>200</td>
<td>1</td>
</tr>
<tr>
<td>Attenuator</td>
<td>-1</td>
<td>30</td>
<td>1</td>
</tr>
<tr>
<td>RFIC</td>
<td>69</td>
<td>-6</td>
<td>7</td>
</tr>
<tr>
<td>GNI Analysis</td>
<td>84</td>
<td>-21.0</td>
<td>10.75</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>-117.8 dBm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4: GNI analysis of Channel-1 for nominal gain.

<table>
<thead>
<tr>
<th>Section</th>
<th>Gain (dB)</th>
<th>IP3 (dBm)</th>
<th>Noise Figure (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiplexer</td>
<td>-4</td>
<td>200</td>
<td>4</td>
</tr>
<tr>
<td>Preamp</td>
<td>25</td>
<td>12.9</td>
<td>2.7</td>
</tr>
<tr>
<td>Filter</td>
<td>-1</td>
<td>200</td>
<td>1</td>
</tr>
<tr>
<td>Attenuator</td>
<td>-5</td>
<td>30</td>
<td>5</td>
</tr>
<tr>
<td>RFIC</td>
<td>69</td>
<td>-6</td>
<td>7</td>
</tr>
<tr>
<td>GNI Analysis</td>
<td>84</td>
<td>-21.0</td>
<td>6.84</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>-120.8 dBm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 5: GNI analysis of Channel-2 for nominal gain.
### Table 6: GNI analysis of Channel-3 for nominal gain.

<table>
<thead>
<tr>
<th>Section</th>
<th>Gain (dB)</th>
<th>IP3 (dBm)</th>
<th>Noise Figure (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiplexer</td>
<td>-1</td>
<td>200</td>
<td>1</td>
</tr>
<tr>
<td>Preamp</td>
<td>25</td>
<td>12.9</td>
<td>2.7</td>
</tr>
<tr>
<td>Filter</td>
<td>-1</td>
<td>200</td>
<td>1</td>
</tr>
<tr>
<td>Attenuator</td>
<td>-8</td>
<td>30</td>
<td>8</td>
</tr>
<tr>
<td>RFIC</td>
<td>69</td>
<td>-6</td>
<td>7</td>
</tr>
<tr>
<td>GNI Analysis</td>
<td>84</td>
<td>-21.0</td>
<td>3.98</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>-127.8</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table 7: GNI analysis of Channel-4 for nominal gain.

<table>
<thead>
<tr>
<th>Section</th>
<th>Gain (dB)</th>
<th>IP3 (dBm)</th>
<th>Noise Figure (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiplexer</td>
<td>-5.0</td>
<td>200</td>
<td>5.0</td>
</tr>
<tr>
<td>Preamp</td>
<td>25</td>
<td>12.9</td>
<td>2.7</td>
</tr>
<tr>
<td>Filter</td>
<td>-1</td>
<td>200</td>
<td>1</td>
</tr>
<tr>
<td>Attenuator</td>
<td>-1.0</td>
<td>30</td>
<td>1.0</td>
</tr>
<tr>
<td>RFIC</td>
<td>66</td>
<td>-6</td>
<td>7</td>
</tr>
<tr>
<td>GNI Analysis</td>
<td>84</td>
<td>-24.0</td>
<td>7.75</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>-125.5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## 4 Description of Multiplexer Section

A four channel multiplexer has been designed using the methodology described in [8]. As we know sensitivity depends on signal to noise ratio and external noise can be very strong in practical scenarios, especially at low frequencies (below 400 MHz). So, when the ratio of external noise to internal noise is large, additional effort to minimize reflection coefficient or internal noise will have little effect on sensitivity. Therefore, our main idea is to design a multiplexer, which may be poorly matched with the antenna impedance, in such a way that the front end is dominated by the external noise and provide acceptable sensitivity.

In our design we use a simple monopole antenna ANT-433-CW from Antenna Factor. The length of this antenna is 17.3 cm long and diameter is 6 mm. The measured impedance of this antenna is shown in Figure 4.

Figure 5 shows the response of the designed multiplexer optimized to match with the antenna impedance to provide acceptable sensitivity. These results are expressed in terms of transducer power gain (TPG), defined as the ratio of power delivered by a matching network to a load, to the power delivered to a perfectly matched load directly from the antenna. Note that the performance is unacceptable, especially in the 138-174 MHz band. However, this poor matching gives us the sensitivity of -117.8 dBm, which is acceptable for our receiver.

Each of the channel of our designed multiplexer uses fifth order chebyshev topology, which is shown in Figure 6. Table 8 shows the component values of multiplexer before and
Figure 4: Antenna impedance.

Figure 5: Multiplexer response.
after the optimization.

![Multiplexer topology of each channel.](image)

**Figure 6: Multiplexer topology of each channel.**

<table>
<thead>
<tr>
<th>Component</th>
<th>Channel–1</th>
<th>Channel–2</th>
<th>Channel–3</th>
<th>Channel–4</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Before</td>
<td>After</td>
<td>Before</td>
<td>After</td>
</tr>
<tr>
<td>L1 (nH)</td>
<td>377.1</td>
<td>306.0</td>
<td>1357.4</td>
<td>1350</td>
</tr>
<tr>
<td>C1 (pF)</td>
<td>2.8</td>
<td>5.4</td>
<td>0.4</td>
<td>0.41</td>
</tr>
<tr>
<td>L2 (nH)</td>
<td>9.7</td>
<td>7.8</td>
<td>1.3</td>
<td>1.32</td>
</tr>
<tr>
<td>C2 (pF)</td>
<td>108.7</td>
<td>139.0</td>
<td>391.4</td>
<td>399</td>
</tr>
<tr>
<td>L3 (nH)</td>
<td>561.6</td>
<td>426.0</td>
<td>2021.9</td>
<td>2027</td>
</tr>
<tr>
<td>C3 (pF)</td>
<td>1.9</td>
<td>2.45</td>
<td>0.3</td>
<td>0.255</td>
</tr>
<tr>
<td>L4 (nH)</td>
<td>9.7</td>
<td>9.0</td>
<td>1.3</td>
<td>1.32</td>
</tr>
<tr>
<td>C4 (pF)</td>
<td>108.7</td>
<td>118.0</td>
<td>391.4</td>
<td>393.0</td>
</tr>
<tr>
<td>L5 (nH)</td>
<td>377.1</td>
<td>246.0</td>
<td>1357.4</td>
<td>1380</td>
</tr>
<tr>
<td>C5 (pF)</td>
<td>2.8</td>
<td>4.33</td>
<td>0.4</td>
<td>0.375</td>
</tr>
</tbody>
</table>

Table 8: Component values of the multiplexer before and after the optimization.

## 5 Description of Amplifier Section

In our design we use GALI-74 amplifier from Minicircuits. This amplifier is chosen mainly for its low cost and low noise characteristics. ADCH-80A, a wideband choke from Minicircuits, is also used to minimize the RF loss caused by the DC biasing resistor. The circuit of this amplifier is designed for 9V DC bias. Fig. 7 shows the circuit diagram example for the amplifier. Detailed circuit diagrams can be found in “Amplifier” sheet in Appendix B. This sheet also contains four fifth order chebyshev bandpass filters after each of the amplifiers to perform additional filtering.

## 6 Description of Attenuator Section

To control the attenuation of the received signal we use a 5-bit digitally controlled attenuator HMC470LP3 from Hittite Microwave Inc. Fig. 8 shows the circuit diagram of the attenuator. Detailed circuit diagrams can be found in “Attenuator” sheet in Appendix B.
Figure 7: Amplifier section (the unconnected line on the left side connects the input port of the amplifier with the RX switches and right side goes to input of the bandpass filter).

Figure 8: Attenuator section (RF1 and RF2 are the input and output port of the attenuator. Other unconnected lines in the figure are the control signal to vary the attenuation).
7 Description of Power Supply Section

One 9V supply voltage for amplifiers and one 5V supply voltage for RF switches and attenuators, have been created from a single 16V power source. This 16V input voltage is fed into a 1.1A low dropout regulator IC LT1965 to create a 9V positive voltage. 5V regulated voltage is supplied by the 500 mA low dropout regulator ICs LT763. Both of these regulator ICs are manufactured by Linear Technology Inc. Detailed circuit diagrams can be found in “Power Supply” sheet in Appendix B.

8 Description of the Settings

Table 9 shows the specification of attenuator control signals to get various attenuation.

<table>
<thead>
<tr>
<th>V1 16dB</th>
<th>V2 8dB</th>
<th>V3 4dB</th>
<th>V4 2dB</th>
<th>V5 1dB</th>
<th>ATT State</th>
</tr>
</thead>
<tbody>
<tr>
<td>High</td>
<td>High</td>
<td>High</td>
<td>High</td>
<td>High</td>
<td>Insertion Loss</td>
</tr>
<tr>
<td>High</td>
<td>High</td>
<td>High</td>
<td>High</td>
<td>Low</td>
<td>1dB</td>
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<tr>
<td>High</td>
<td>High</td>
<td>Low</td>
<td>High</td>
<td>High</td>
<td>2dB</td>
</tr>
<tr>
<td>High</td>
<td>Low</td>
<td>High</td>
<td>High</td>
<td>High</td>
<td>4dB</td>
</tr>
<tr>
<td>Low</td>
<td>High</td>
<td>High</td>
<td>High</td>
<td>High</td>
<td>8dB</td>
</tr>
<tr>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>16dB</td>
</tr>
<tr>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>31dB</td>
</tr>
</tbody>
</table>

Table 9: Attenuator control signals.

Table 10 shows the Rx/Tx switch control signals.

<table>
<thead>
<tr>
<th>S0</th>
<th>S1</th>
<th>Rx/Tx Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>High</td>
<td>X</td>
<td>RX Mode</td>
</tr>
<tr>
<td>Low</td>
<td>Low</td>
<td>TX Mode ( Ch.1 or Ch.3 )</td>
</tr>
<tr>
<td>Low</td>
<td>High</td>
<td>TX Mode ( Ch.2 or Ch.4 )</td>
</tr>
</tbody>
</table>

Table 10: Rx/Tx Switch Control Signals.

9 Summary

A summary of the cost for one RFFE board is given in Table 11. Since we prepared just two boards for the present study using the quickest manufacturing time, the PCB fabrication and assembly cost is not representative of the cost to build the same device in large quantities.
<table>
<thead>
<tr>
<th>Component</th>
<th>Quantity</th>
<th>Price (US $)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Regulator ICs</td>
<td>2</td>
<td>8.58</td>
</tr>
<tr>
<td>Amplifier</td>
<td>4</td>
<td>18.80</td>
</tr>
<tr>
<td>RF Choke</td>
<td>4</td>
<td>59.0</td>
</tr>
<tr>
<td>Attenuator</td>
<td>4</td>
<td>15.32</td>
</tr>
<tr>
<td>RF Switch</td>
<td>6</td>
<td>7.08</td>
</tr>
<tr>
<td>Capacitor</td>
<td>109</td>
<td>16.35</td>
</tr>
<tr>
<td>Inductor</td>
<td>61</td>
<td>45.75</td>
</tr>
<tr>
<td>Resistor</td>
<td>7</td>
<td>1.00</td>
</tr>
<tr>
<td>MMCX Connector</td>
<td>6</td>
<td>60.30</td>
</tr>
<tr>
<td>Other Connectors</td>
<td>5</td>
<td>10.0</td>
</tr>
<tr>
<td>Other Components</td>
<td>3</td>
<td>3.50</td>
</tr>
<tr>
<td><strong>Subtotal</strong></td>
<td></td>
<td><strong>245.68</strong></td>
</tr>
<tr>
<td>PC Board</td>
<td>1</td>
<td>450.00</td>
</tr>
<tr>
<td>PC Board Assembly</td>
<td>1</td>
<td>925.00</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td><strong>1620.68</strong></td>
</tr>
</tbody>
</table>

Table 11: Summary of the cost for one RFFE board.
References


Appendices
A Bill of Materials

This section presents the bill of materials.
<table>
<thead>
<tr>
<th>Item</th>
<th>Qty</th>
<th>Reference</th>
<th>Part Name</th>
<th>Package</th>
<th>Manufacturer</th>
<th>Manufacturer Part#</th>
<th>Distributor</th>
<th>Distributor Part#</th>
<th>Description</th>
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<td>1</td>
<td>U1</td>
<td>74VHCT04AMTC</td>
<td>14-TSSOP</td>
<td>FAIRCHILD</td>
<td>74VHCT04AMTC</td>
<td>Mouser</td>
<td>512-74VHCT04AMTC</td>
<td>HEX INVERTER</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>L21 L27 L33 L39</td>
<td>ADCH-80A</td>
<td>D542</td>
<td>Minicircuits</td>
<td>ADCH-80A+</td>
<td>Minicircuits</td>
<td>ADCH-80A+</td>
<td>RF Choke</td>
</tr>
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<td>1</td>
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<td>0.01uF 100V</td>
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<td>12101C103KAT2A</td>
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<tr>
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<td>478-2570-1-ND</td>
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</tr>
<tr>
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</tr>
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<td>0.6pF 250V</td>
<td>CAP_0603</td>
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<td>SQCSVA0R6BAT1A</td>
<td>Digikey</td>
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<td>SURFACE MOUNT CAPACITOR 0.098 X 0.126 INCHES</td>
</tr>
<tr>
<td>10</td>
<td>4</td>
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<td>0.7pF 50V</td>
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<td>AVX Corporation</td>
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</tr>
<tr>
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<tr>
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</tr>
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<td>15</td>
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<td>1.8pF 250V</td>
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<td>SQCSVA1R8BAT1A</td>
<td>Digikey</td>
<td>478-3490-1-ND</td>
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</tr>
<tr>
<td>16</td>
<td>14</td>
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</tr>
<tr>
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<td>Linear Regulator</td>
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</table>
B Schematic

This section presents the schematic of the RFFE board. This schematic contains the following four pages:

- Multiplexer and Switch Circuits
- Amplifier Circuits
- Attenuator Circuits
- Power Supply Circuits
C Layout

This section presents the layout and component placement of the RFFE board. The pages are added in the following order -

- Top layer (primary component side)
- Bottom layer (secondary component side)
- First inner layer (power layer)
- Second inner layer (ground layer)
- Component placement in top layer, and
- Component placement in bottom layer.
Revision of the RFIC Board for NIJ Public Safety Radio

S.M. Shajedul Hasan* and S.W. Ellingson

July 22, 2008

Contents

1 Introduction 2
2 Revised Design 2
3 Summary 3
A Bill of Materials 8
B Schematic 12
C Layout 19

*Bradley Dept. of Electrical & Computer Engineering, 432 Durham Hall, Virginia Polytechnic Institute & State University, Blacksburg, VA 24061 USA. E-mail: hasan@vt.edu
1 Introduction

In [1], we presented the design and development of an evaluation board with RFIC “Version 4”. This board was developed under multi-band/multi-mode radio (MMR) project in Virginia Tech sponsored by the U.S. Department of Justice [2]. A prototype radio was built using this RFIC board to demonstrate the basic functionality of our desired MMR [3]. After the successful integration of the first prototype we planned to build a another prototype MMR, which will be more compact and will have less cable connections. Hence, we revised our first version of RFIC board. This report presents the overall description of the revised RFIC board. The image of this board is shown in Figure 1.

Figure 1: Image of RFIC board.

This report is organized as follows. Section 2 presents the summary of the changes we made from the previous version of RFIC. Section 3 concludes the report presenting the total cost. Finally, three appendices present the bill of materials, complete schematic and layout images.

2 Revised Design

The following changes have been made in this revised RFIC board:

- Removed all the power jumpers
- Added Receive and Transmit AGC circuits
- Added MMCX ganged connectors
- Corrected Power Supply Circuits
• Added connectors for supplying power to board to board

Table 1 present all the input/output ports of the revised RFIC board.

3 Summary

A summary of the cost for one RFFE board is given in Table 2. Since we prepared just two boards for the present study using the quickest manufacturing time, the PCB fabrication and assembly cost is not representative of the cost to build the same device in large quantities.
<table>
<thead>
<tr>
<th>Function</th>
<th>Port Name</th>
<th>Conn. Name</th>
<th>Characteristics</th>
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<tbody>
<tr>
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<td>J61</td>
<td>RF input, 100 MHz to 2.5 GHz</td>
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<tr>
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<td>RX-2</td>
<td>J60</td>
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<td>RX-3</td>
<td>J59</td>
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<td>RX-4</td>
<td>J58</td>
<td></td>
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<tr>
<td></td>
<td>RX-5</td>
<td>J62</td>
<td>RF input, 500 MHz to 2.5 GHz</td>
</tr>
<tr>
<td>Tx RF Output</td>
<td>TX-1</td>
<td>J52</td>
<td>RF Output, 100 MHz to 1000 MHz</td>
</tr>
<tr>
<td></td>
<td>TX-2</td>
<td>J54</td>
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</tr>
<tr>
<td></td>
<td>TX-3</td>
<td>J56</td>
<td>RF Output, 500 MHz to 2.5 GHz</td>
</tr>
<tr>
<td>Rx Baseband Output</td>
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<td>J4-A</td>
<td>Baseband in-phase differential signal output</td>
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<tr>
<td></td>
<td>RX_BB_In</td>
<td>J4-B</td>
<td></td>
</tr>
<tr>
<td></td>
<td>RX_BB_Qp</td>
<td>J4-C</td>
<td>Baseband quadrature-phase differential signal output</td>
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<tr>
<td></td>
<td>RX_BB_Qn</td>
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<td>Tx Baseband Input</td>
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<td>J3-A</td>
<td>In-phase differential signal max. 2V peak-peak</td>
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<tr>
<td></td>
<td>TX_BB_In</td>
<td>J3-B</td>
<td></td>
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<tr>
<td></td>
<td>TX_BB_Qp</td>
<td>J3-C</td>
<td>Quadrature-phase differential signal max. 2V peak-peak</td>
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<tr>
<td></td>
<td>TX_BB_Qn</td>
<td>J3-D</td>
<td></td>
</tr>
<tr>
<td>Freq. Reference Input</td>
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<td>J12</td>
<td>External LO input to the mixer</td>
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<td>J24</td>
<td>1GHz external input used when bypassing the PLL</td>
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<td></td>
<td>FREF</td>
<td>J15</td>
<td>31.25 MHz reference for PLL</td>
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<td>J1-A</td>
<td>DDS Rx positive calibration output</td>
</tr>
<tr>
<td></td>
<td>QLOP-A</td>
<td>J1-B</td>
<td>DDS Rx negative calibration output</td>
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<td></td>
<td>ILON-A</td>
<td>J1-C</td>
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</tr>
<tr>
<td></td>
<td>ILOP-A</td>
<td>J1-D</td>
<td>DDS Tx forward negative calibration output</td>
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<td>QLON-B</td>
<td>J2-A</td>
<td>DDS Tx feedback positive calibration output</td>
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<td>J2-B</td>
<td>DDS Tx feedback negative calibration output</td>
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<td></td>
<td>ILON-B</td>
<td>J3-C</td>
<td>DDS Tx feedback differential positive output</td>
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<td>ILOP-B</td>
<td>J3-D</td>
<td>DDS Tx feedback differential negative output</td>
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<td>TX_AGC</td>
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<td>Transmit AGC enable/disable</td>
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<td>RX AGC Enable</td>
<td>RX_AGC</td>
<td>J8</td>
<td>Receive AGC enable/disable</td>
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<td>SPI</td>
<td>SPI</td>
<td>J41</td>
<td>serial port interface to PC</td>
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<tr>
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<td>PWR</td>
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<td>Power Supply Input</td>
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Table 1: Input/Output ports of the RFIC board.
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</table>

Table 2: Summary of the cost for one RFIC board. (*The cost of the RFIC is a very rough estimate provided by Motorola.*)
References


Appendices
A  Bill of Materials

This section presents the bill of materials.
<table>
<thead>
<tr>
<th>Item</th>
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B Schematic

This section presents the schematic of the RFIC board. This schematic contains the following six pages-

- Main
- Baseband IO
- SPI IO
- RX_RF_IO
- TX_RF_IO
- Power Supply
C Layout

This section presents the layout and component placement of the RFFE board. The pages are added in the following order -

- Top layer (primary component side)
- Bottom layer (secondary component side)
- First inner layer (power layer)
- Second inner layer (ground layer)
- Component placement in top layer, and
- Component placement in bottom layer.
Revision of the ADC/DAC Board for NIJ Public Safety Radio

S.M. Shajedul Hasan* and S.W. Ellingson

July 22, 2008

Contents

1 Introduction 2
2 Revised Design 2
3 Summary 3
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B Schematic 11
C Layout 16

*Bradley Dept. of Electrical & Computer Engineering, 432 Durham Hall, Virginia Polytechnic Institute & State University, Blacksburg, VA 24061 USA. E-mail: hasan@vt.edu
1 Introduction

In [1], we presented the design and development of an ADC/DAC evaluation board for NIJ public safety radio. This board was developed under multi-band/multi-mode radio (MMR) project in Virginia Tech sponsored by the U.S. Department of Justice [2]. A prototype radio was built using this ADC/DAC board to demonstrate the basic functionality of our desired MMR [3]. After the successful integration of the first prototype we planned to build another prototype MMR, which will be more compact and will have less cable connections. Hence, we revised our first version of ADC/DAC board. This report presents the overall description of the revised ADC/DAC board. The image of this board is shown in Figure 1.

![Image of ADC/DAC board.](image)

Figure 1: Image of ADC/DAC board.

This report is organized as follows. Section 2 presents the summary of the changes we made from the previous version of RFIC. Section 3 concludes the report presenting the total cost. Finally, three appendices present the bill of materials, complete schematic and layout images.

2 Revised Design

The following changes have been made in this revised RFIC board:

- Removed all the power jumpers
- Added MMCX ganged connectors
- Revised power supply circuits
- Added synthesizer circuits

Table 1 presents all the input/output ports of the revised RFIC board.

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<tr>
<th>Function</th>
<th>Port Name</th>
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<th>Characteristics</th>
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<td>IB</td>
<td>J8-A</td>
<td>Differential Output</td>
</tr>
<tr>
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<td>IA</td>
<td>J8-B</td>
<td>of I-Channel</td>
</tr>
<tr>
<td></td>
<td>QB</td>
<td>J8-C</td>
<td>Differential Output</td>
</tr>
<tr>
<td></td>
<td>QA</td>
<td>J8-D</td>
<td>of Q-Channel</td>
</tr>
<tr>
<td>ADC Input</td>
<td>IA</td>
<td>J24-A</td>
<td>Differential Input</td>
</tr>
<tr>
<td></td>
<td>IB</td>
<td>J24-B</td>
<td>of I-Channel</td>
</tr>
<tr>
<td></td>
<td>QB</td>
<td>J24-C</td>
<td>Differential Input</td>
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<tr>
<td></td>
<td>QA</td>
<td>J24-D</td>
<td>of Q-Channel</td>
</tr>
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<td>CLK_ADC</td>
<td>J5</td>
<td>ADC Reference Clock</td>
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<td>EXT_CLK</td>
<td>J9</td>
<td>External DAC Clock</td>
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<td>RF_OUT</td>
<td>J27</td>
<td>RF output from the synthesizer</td>
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<tr>
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<td>J1, J12</td>
<td>ADI interface to FPGA</td>
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</table>

Table 1: Input/Output ports of the ADC/DAC board.

3 Summary

A summary of the cost for one ADC/DAC board is given in Table 2. Since we prepared just two boards for the present study using the quickest manufacturing time, the PCB fabrication and assembly cost is not representative of the cost to build the same device in large quantities.
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<td><strong>1667.20</strong></td>
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Table 2: Summary of the cost for one ADC/DAC board.
References


Appendices
A Bill of Materials

This section presents the bill of materials.
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<tr>
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<td>R36 R40</td>
<td>100 1/10W</td>
<td>RES-0603</td>
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<td>ERU-3GEYJ101V</td>
<td>Diigkey</td>
<td>PI00GCT-ND</td>
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<td>Distributor</td>
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<td>Mouser</td>
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</table>
B Schematic

This section presents the schematic of the ADC/DAC board. This schematic contains the following four pages-

- ADC Circuits
- DAC Circuits
- Power Supply Circuits
- Synthesizer Circuit
C  Layout

This section presents the layout and component placement of the RFFE board. The pages are added in the following order -

• Top layer (primary component side)
• Bottom layer (secondary component side)
• First inner layer (power layer)
• Second inner layer (ground layer)
• Component placement in top layer, and
• Component placement in bottom layer.
User Interface for NIJ Public Safety Radio

Qian Liu, Rithirong Thandee, S.M. Hasan and S.W. Ellingson

October 22, 2008

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1 Introduction

The Gumstix LCD pack [KIT0019]¹ is used as the user interface for choosing the frequency of the VT NIJ public safety radio². This report describes its architecture, the software for graphic display and command dispatch, installation instructions for people who wish to study this work, some discussion of issues about how to modify the software for further development, and the user guide for people who would like to use this interface. To provide context, Figure 1 shows a conceptual block diagram of the prototype.

![Figure 1: Block Diagram](image)

This report is organized as follows. Section 2 describes assembly of the Gumstix LCD pack and details the interfaces between the Gumstix and the RFIC board as well as the Gumstix and the FPGA board. Section 3 presents the software development kit. Section 4 discusses the application programs. Section 5 summarize the instruction to use the graphic interface. Finally, two appendices present the source code and troubleshooting information.

²[http://www.ece.vt.edu/swe/chamrad/](http://www.ece.vt.edu/swe/chamrad/)
2 Description of Hardware Development Kit

2.1 Gumstix LCD Pack Assembly

Figure 2 presents all the components of the LCD pack used in this report.

![Gumstix LCD Pack](image)

Connect the LCD panel directly to the consoleLCD16-vx board first. Then, the netmicroSD expansion board must be securely connected to the verdex motherboard with a good pressure. Be sure that the pressure is applied only at the indicated locations printed on the verdex motherboard. It is time to attach the verdex motherboard to the consoleLCD16-vx expansion board. Finally, use screws and spacers kit to make them fixed. The online Flash animates the assembly procedure, and Figure 3 shows the model.

Since the LCD pack uses the verdex motherboard, the middle port of the three RS232 ports on miniDIN8 connectors on the consoleLCD16-vx should be used to connect to the serial port on the development machine (a desktop or laptop) through the null-modem serial cable, as Figure 1 shown. If the development machine has no open serial port, a USB serial adaptor is needed to connect to the null-modem serial cable and to the USB port on the development machine.

2.2 SPI Communication

This report uses the "bit banging" method to control the serial peripheral interface (SPI); that is, the master (Gumstix) uses the general-purpose
input/output (GPIO) pins to generate slave select signals in the given time intervals. Generally, data can be transferred in both directions simultaneously when the slave select signal is low active. However, SPI communication in this report is only one way at current stage. That is why the signal MISO in Figure 4 is connected with the dotted line. The signal RESET in Figure 4 is not defined in SPI bus, but it is required by the RFIC chip as the reset operation is needed before reprogramming the RFIC chip.

<table>
<thead>
<tr>
<th>Gumstix (Master)</th>
<th>RFIC (Slave)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>RESET</td>
<td>RESET</td>
</tr>
<tr>
<td>CHIP_S</td>
<td>SS*</td>
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<tr>
<td>MISO</td>
<td>MISO</td>
</tr>
<tr>
<td>DATA</td>
<td>MOSI</td>
</tr>
<tr>
<td>CLK</td>
<td>SCLK</td>
</tr>
</tbody>
</table>

Figure 4: SPI communication between Gumstix and RFIC

The Gumstix selects a channel and sends the corresponding channel information to the FPGA board. The FPGA board processes the channel
information and then sends them to the RF Front End (RFFE) board [1]. The signals CH_A and CH_B in Figure 5 controls the channel selection. Table 1 is the true table for the channel selection, and the details of the channel information can be found in [1].

Table 1: Channel Selection True Table

<table>
<thead>
<tr>
<th>Control Signals</th>
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<tr>
<td>CH_A</td>
<td>CH_B</td>
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<tr>
<td>Low</td>
<td>Low</td>
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<tr>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>High</td>
<td>High</td>
</tr>
</tbody>
</table>

Figure 5: Connection between Gumstix and FPGA

2.3 GPIO Pin Allocation

Figure 6 shows the GPIO expansion interface on the consoleLCD_16vx board in the view of the bottom layer. This report has used SPI port (NSSP) for the SPI communication with the RFIC board [2, 3], and BlueTooth UART (BTUART) to send the channel information signals to the FPGA board.

According to the GPIO characteristics [4] and GPIO pin positions in Figure 6, Table 2 presents the GPIO pin mapping.
Figure 6: PCB Bottom-Side Silkscreen of consoleLCD_16vx Board

http://pubs.gumstix.org/boards/CONSOLE/LCD16/PCB10016-R1833/PCB10016.bot.png

Table 2: GPIO Pin Definition

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Signal Name</th>
</tr>
</thead>
<tbody>
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<td>J14-6</td>
</tr>
<tr>
<td>GPIO&lt;11&gt;</td>
<td>NSSP-2</td>
<td>J14-2</td>
</tr>
<tr>
<td>GPIO&lt;14&gt;</td>
<td>NSSP-3</td>
<td>J14-5</td>
</tr>
<tr>
<td>GPIO&lt;19&gt;</td>
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<td>J14-4</td>
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<tr>
<td>GPIO&lt;45&gt;</td>
<td>BTUART-5</td>
<td>J27-9</td>
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<tr>
<td>GPIO&lt;46&gt;</td>
<td>BTUART-6</td>
<td>J27-11</td>
</tr>
</tbody>
</table>

*They are for the Gumstix.

*bRefers to [2] for the pin information.

*cRefers to [5] for the pin information.
3 Description of Software Development Kit

3.1 Getting Started

3.1.1 Prerequisites

A computer running a fairly recent Linux distribution, such as Ubuntu 7.10, with at least 10 GB of free space on the hard drive is needed as the development machine. It is better that the development machine has an open serial port. If not, a USB-serial converter is required for the connection. Also an internet connection should be available for downloading packages and source code.

Run “apt-get install” in the terminal or use the package management tool to install the following packages: gcc, patch, help2man, diffstat, texi2html, makeinfo, ncurses-devel, cvs, gawk, python-dev, and python-pysqlite2.

This report uses an Ubuntu distribution, so it is necessary to change /bin/sh to link to /bin/bash. The method is to run “sudo dpkg-reconfigure dash”, and answer no when asked whether you want to install dash as /bin/sh.

3.1.2 Setting Up a Build Environment

The online documentation gives instructions to set up a build environment. For this report, the build environment can be set up as follows:

```
$ svn –version
$ mkdir ~/gumstix
$ cd ~/gumstix
$ svn co https://gumstix.svn.sourceforge.net/svnroot/gumstix/trunk gumstix-oe
$ cat gumstix-oe/extras/profile >> ~/.bashrc
$ sudo groupadd oe
$ sudo username -a -G oe username.
$ mkdir /usr/share/sources
$ chgrp oe /usr/share/sources
$ chmod 0775 /usr/share/sources
```

[^3]: <http://www.gumstix.net/Software/view/Getting-started/111.html>

[^4]: It is the username of the login account to the Linux distribution on the development machine.
$ chmod ug+s /usr/share/sources

Now close the terminal window and open a new one to make the above environment changes take effect. In the new window, run “bitbake gumstix-basic-image” to build a basic root file system image. Depending on the downloading speed, it will take about six hours or more to download all the source code for the initial build. When it completes, the root file system image and the kernel image can be found by running “ls -l ~/gumstix/gumstix-oe/tmp/deploy/glibc/images/gumstix-custom-verdex/”.

### 3.1.3 Setting Up a Serial Connection

First run “sudo apt-get install cKermit” to install Kermit communication package. Then, follow online instructions\(^5\) to set up the serial connection.

```
$ kermit -l /dev/ttyUSB0
C-Kermit> take ~/gumstix/gumstix-oe/extras/kermit-setup
C-Kermit> connect
```

When the Gumstix LCD pack has been connected and powered on, a message from U-Boot followed by the normal Gumstix boot sequence can be seen in the terminal window, showing the serial connection has been set up successfully.

### 3.2 Creating a Bootable microSD Card

This reports uses the X Window system (commonly X11 or X) to provide the standard toolkit and protocol with which to build graphical user interfaces (GUIs) in Ubuntu\(^6\). Considering the large memory size needed for the X11 and limited memory size of the on-board flash, an external 2 GB microSD card is used to store the Linux boot image, the root file image, and application program. In this case, the Gumstix boots from the microSD card, which has nothing to do with the existing U-Boot, rootfs, or kernel images in the on-board flash.

\(^5\)http://www.gumstix.net/Software/view/Getting-started/Setting-up-a-serial-connection/111.html

3.2.1 Repartitioning the microSD Card

First insert the card into the development machine’s flash card slot. A microSD to SD card adaptor may be needed to fit the development machine’s flash card slot. Assume that the newly inserted card shows up as /dev/sde1. Then it is necessary to unmount the card’s existing file system by running “sudo umount /dev/sde1” before getting started to repartition the card. There are a couple ways to partition the memory disk. One way is to run “fdisk” to partition the card, and then run “mkfs.vfat” and “mkfs.ext2” to format the partitions as a FAT file system and an ext2 file system respectively. However, such methods do not always work. This report uses a GUI partitioning tool, GParted, to partition and format the microSD card.

If GParted is not installed on the development machine, run “sudo apt-get install gparted” firstly. When completed, use “gparted” to launch the program, and select the media (sde1) to partition it into two partitions as a FAT16 partition and an ext2 partition. The FAT16 partition with the size of 80 MB only places the boot script and linux boot image (uimage), and the ext2 partition uses the rest of the available space of the microSD card for the root file system and application program.

3.2.2 Installing the Boot Files

Two files, gumstix-factory.script and uimage, are required on the FAT16 partition to boot the X11. Download and extract the kernel image to the FAT16 partition by the following procedure:

```
$ cd /media/disk
$ wget http://www.sakoman.net/oe/mmc-boot/kernel-mmc.tar.gz
$ sudo tar xvf kernel-mmc.tar.gz
$ sudo rm kernel-mmc.tar.gz
```

Using the same method, download and extract the rootfs image to the ext2 partition as follows:

```
$ cd /media/disk-1
$ wget http://www.sakoman.net/oe/mmc-boot/rootfs-mmc.tar.gz
```

8Assume the FAT16 partition is mounted as disk
9Assume the ext2 partition is mounted as disk-1
$ sudo tar xvf rootfs-mmc.tar.gz
$ sudo rm rootfs-mmc.tar.gz

When completed, it is very important to unmount the two file systems before placing the microSD card into the slot on the Gumstix board. Skipping this step will corrupt the card data and make booting fail. After transferring the microSD card to the Gumstix board and powering it up, the Gumstix can run with the root file system on the microSD card.

3.3 Transferring files through Ethernet

It is more convenient to debug the application programs on the development machine, and then transfer them to the microSD card after the successful compilation and debugging.

3.3.1 IP Address Configuration

Due to the high speed, the Ethernet cable with a router is an ideal way to copy files on the Gumstix. However, the file transfer will fail if the IP address of the development machine is higher than that of the Gumstix. To solve this problem, run `ifconfig` to change the IP address of either the development machine or the Gumstix. Take the Gumstix as an example. We log into the Gumstix first, and then run the following command

```
ifconfig eth0 192.168.1.103
```

to set the Gumstix’s IP address to 192.168.1.103. The development machine’s IP address can also be changed in the same way through a terminal window on the development machine.

3.3.2 Transfer Command

When the IP address of the development machine is lower than that of the Gumstix, the file can be transferred successfully with the commands, cp, rcp, scp, and so on. This report uses the secure copy (scp) command to transfer files in a remote and secure mode. After changing directory to that of the file which will be transferred, the following command

```
scp program_name_exe root@192.168.1.103:/home/root
```

can copy the file `program_name_exe` to the fold `root` in the home directory of the Gumstix.

\(^{10}\)Generally, eth0 represents the LAN ethernet connection, and eth1 denotes the wireless connection.
4 Application Program Discussion

The application program is divided into two parts as SPI code and Python program, and all the source code can be found in Appendix A.

4.1 SPI Code

The SPI code is written in C language, and is called by Python to send SPI signals through the GPIO pins to command the NIJ radio.²

4.1.1 GPIO Configuration

The GPIOs are programmed by the functions distributed by the Free Software Foundation. The following functions represent how to configure the GPIOs.

Function “gpio(OUT, SET, 59);” programs GPIO<59> as a GPIO function, sets its direction as output and sets it to a logic 1.

Function “gpio_function(59, GPIO);” programs GPIO<59> as a GPIO function.

Function “gpio_direction(59, OUT);” program GPIO<59> as an output.

Function “gpio_set(59);” programs GPIO<59> to a logic 1.

Function “gpio_clear(59);” programs GPIO<59> to a logic 0.

Command “i = gpio_status(59);” makes i be set to the logic level of GPIO<59>.

4.1.2 Data Format Conversion

The data and address read from the file are in hexadecimal format; however, SPI bus is serial. Hence, the function putBin( ) is used to convert the hexadecimal data into binary format. The source code can be found in Appendix A.

4.1.3 Program Flow

Figure 7 shows how the Gumstix sends data to reprogram the RFIC through its GPIOs according to the SPI bus protocol. The clock for the SPI
communication is software-programmed, so the transfer speed depends on the program execution speed.

![Flow Chart](image)

Figure 7: Flow Chart

### 4.2 Python Program

In this report, the Python program uses basic functions to create four buttons for the frequency choice. When the user presses a button, the Python program will call a C program with an argument, which will read the script file and then send SPI signal through GPIOs to tell the RFIC board which frequency has been selected.

Importing two Python modules as `os` and `sys`, the following command

```python
os.system("./myprogram myargument")
```

can call a C program `myprogram` with an argument `myargument`. In this way, everything inside the quotation is executed as if from the command line.

The GUI can be easily changed by resetting the parameters of the functions such as `window.set_border_width()`, `window.set_size_request()`, and so
on[6]. For example, the function `windown.set_size_request(480, 272)` creates a window with size of $480 \times 272$. The other settings can all be configured in the same way, and the details are explained in Appendix A.

Figure 8 shows the touchscreen interface for the VT NIJ public safety radio. The buttons are used for the user to choose a desired frequency. When the user touches a button, the button will whiten, and the corresponding data will be sent to the RFIC board.

![Touchscreen Interface](image)

**Figure 8: Touchscreen Interface**

### 5 User Guide

Once implemented, the Gumstix user interface operates as follows. Upon power-up, the Gumstix boots from the microSD card, and then the X11 will appear on the screen.

Now a touchstick is used to open the terminal window which is on the left of the taskbar, and then the USB keyboard is used to input the following commands to run the Python.

```
$ cd /home/root
$ python radio.py
```

When finished, the interface shown in Figure 8 will display on the LCD.
Acknowledgment

The authors are thankful to Philip Balister of OpenSDR for providing X Window operating system and patient support to answer the Gumstix related questions.

References


Appendices

A  Program Codes

A.1  SPI Code

/**************************************************************/
/* Copyright©2006 Time Crawford <timcrawford@comcast.net>*/
/* Modified by Rithirong Thandee <rthandee@vt.edu> on April, 2008*/
/* Modified by S.M. Hasan <hasan@vt.edu> on July, 2008*/
/**************************************************************/
#include <stdio.h>
#include <time.h>
#include <stdio.h>
#include <unistd.h>
#include <stdlib.h>
#include <string.h>
#include <sys/mman.h>
#include <sys/types.h>
#include <sys/stat.h>
#include <fcntl.h>
#include <ctype.h>

//========= GPIO Controller Register ========
#define GPLR0 0x40E00000
#define GPLR1 0x40E00004
#define GPLR2 0x40E00008
#define GPDR0 0x40E0000C
#define GPDR1 0x40E00010
#define GPDR2 0x40E00014
#define GPSR0 0x40E00018
#define GPSR1 0x40E0001C
#define GPSR2 0x40E00020
#define GPCR0 0x40E00024
#define GPCR1 0x40E00028
#define GPCR2 0x40E0002C
#define GAFR0_L 0x40E00054
#define GAFR0_U 0x40E00058
#define GAFR1_L 0x40E0005C
#define GAFR1_U 0x40E00060
# define GAFR2_L 0x40E00064
# define GAFR2_U 0x40E00068

// ================================
# define MAP_SIZE 4096
# define MAP_MASK (MAP_SIZE-1)
# define IN 250
# define OUT 251
# define GPIO 0
# define AF0 0
# define AF1 1
# define AF2 2
# define AF3 3
# define SET 252
# define CLEAR 253

// ======= GPIO pins number for SPI ========
# define DATA 13
# define CLK 19
# define CHIP_S 14
# define RESET 11

// ==== GPIO pins number for Channel Information ====
# define CH_A 44
# define CH_B 45

typedef unsigned int u32;
void *map, *regaddr;
void putBin(int type, int digit, int val, char bin[]);

static void putmem(u32 addr, u32 val)
{
    regaddr = (void*)((u32)map + (addr & MAP_MASK));
    *(u32*)regaddr = val;
}

static int getmem(u32 addr)
{
    u32 val;
    regaddr = (void*)((u32)map + (addr & MAP_MASK));
    val = *(u32*)regaddr;
    return val;
}
void gpio_set(u32 gpio) 
{
    u32 pos;
    u32 bit = 1;
    pos = gpio / 32;
    bit <<= gpio % 32;
    putmem(GPSR0 + (pos*4), bit);
}

void gpio_clear(u32 gpio) 
{
    u32 pos;
    u32 bit = 1;
    pos = gpio / 32;
    bit <<= gpio % 32;
    putmem(GPCR0 + (pos * 4), bit);
}

u32 gpio_status(u32 gpio) 
{
    u32 pos;
    u32 bit = 1;
    u32 data;
    pos = gpio / 32;
    bit <<= gpio % 32;
    data = getmem(GPLR0 + (pos * 4));
    data &= bit;
    if(data == 0)
        return(0);
    else
        return(1);
}

void gpio_direction(u32 gpio, u32 dir) 
{
    u32 pos;
    u32 bit = 1;
    u32 data;
    pos = gpio / 32;
    bit <<= gpio % 32;
    data = getmem(GPDR0 + (pos * 4));
}
data &= bit;
if(dir==OUT)
    data |= bit;
    putmem(GPDR0 + (pos * 4), data);
}

void gpio_function(u32 gpio, u32 fun)
{
    u32 pos;
    u32 bit = 3;
    u32 data;
    pos = gpio / 16;
    bit <<= (gpio % 16) * 2;
    fun <<= (gpio % 16) * 2;
    data = getmem(GAFR0_L + (pos * 4));
    data &= bit;
    data |= fun;
    putmem(GAFR0_L + (pos * 4), data);
}

u32 gpio(u32 dir, u32 set, u32 reg)
{
    if((dir != IN) & (dir != OUT)) {
        printf(“ERROR: must specify a valid direction\n”);
        return(1);
    }
    if((set != SET) & (set != CLEAR)) {
        printf(“ERROR: must specify a valid level\n”);
        return(1);
    }
    if(reg > 84) {
        printf(“ERROR: not a valid register -> %d\n”, reg);
        return(1);
    }
    gpio_function(reg, GPIO);
    gpio_direction(reg, dir);
    if(dir == OUT){
        if(set == SET)
            gpio_set(reg);
        else
            gpio_clear(reg);
void putBin(int type, int digit, int val, char bin[]) {
    int one = 0;
    int two = 0;
    int three = 0;
    int four = 0;
    if(type == 1) {
        if(digit == 1) {
            four = 13; three = 12; two = 11; one = 10;
        }
        else if(digit == 2) {
            four = 9; three = 8; two = 7; one = 6;
        }
        else if(digit == 3) {
            four = 5; three = 4; two = 3; one = 2;
        }
        else if(digit == 4) {
            four = 1; three = 0;
        }
    }
    else if(type == 2) {
        if(digit == 1) {
            four = 7; three = 6; two = 5; one = 4;
        }
        else if(digit == 2) {
            four = 3; three = 2; two = 1; one = 0;
        }
    }
    return;
}
if(val=='0')
{
    if(digit!=4) {bin[one]='0';bin[two]='0';}
    bin[three] = '0'; bin[four] = '0';
}
else if(val=='1')
{
    if(digit!=4) {bin[one]='0';bin[two]='0';}
    bin[three] = '0'; bin[four] = '1';
}
else if(val=='2')
{
    if(digit!=4) {bin[one]='0';bin[two]='0';}
    bin[three] = '1'; bin[four] = '0';
}
else if(val=='3')
{
    if(digit!=4) {bin[one]='0';bin[two]='0';}
    bin[three] = '1'; bin[four] = '1';
}
else if(val=='4')
{
    if(digit!=4) {bin[one]='0';bin[two]='1';}
    bin[three] = '0'; bin[four] = '0';
}
else if(val=='5')
{
    if(digit!=4) {bin[one]='0';bin[two]='1';}
    bin[three] = '0'; bin[four] = '1';
}
else if(val=='6')
{
    if(digit!=4) {bin[one]='0';bin[two]='1';}
    bin[three] = '1'; bin[four] = '0';
}
else if(val=='7')
{
    if(digit!=4) {bin[one]='0';bin[two]='1';}
    bin[three] = '1'; bin[four] = '1';
}
else if(val=='8')
{  
  if(digit!=4) {bin[one] = '1'; bin[two] = '0';}
  bin[three] = '0'; bin[four] = '0';
}
else if(val=='9')
{
  if(digit!=4) {bin[one] = '1'; bin[two] = '0';}
  bin[three] = '0'; bin[four] = '1';
}
else if(val=='A' || val == 'a')
{
  if(digit!=4) {bin[one] = '1'; bin[two] = '0';}
  bin[three] = '1'; bin[four] = '0';
}
else if(val=='B' || val == 'b')
{
  if(digit!=4) {bin[one] = '1'; bin[two] = '0';}
  bin[three] = '1'; bin[four] = '1';
}
else if(val=='C' || val == 'c')
{
  if(digit!=4) {bin[one] = '1'; bin[two] = '1';}
  bin[three] = '0'; bin[four] = '0';
}
else if(val=='D' || val == 'd')
{
  if(digit!=4) {bin[one] = '1'; bin[two] = '1';}
  bin[three] = '0'; bin[four] = '1';
}
else if(val=='E' || val == 'e')
{
  if(digit!=4) {bin[one] = '1'; bin[two] = '1';}
  bin[three] = '1'; bin[four] = '0';
}
else if(val=='F' || val == 'f')
{
  if(digit!=4) {bin[one] = '1'; bin[two] = '1';}
  bin[three] = '1'; bin[four] = '1';
}
int main(int argc, char *argv[]) {
    // take the argument determining the file i’m opening
    printf("the argument is %\n", argv[1]);
    // setting up for bit-banging GPIO
    unsigned int iii, ii, rval, speed, count, tmp;
    int fd;
    fd = open("/dev/mem", O_RDWR | O_SYNC);
    if(fd<0) {
        perror("open("/dev/mem")");
        exit(1);
    }
    map = mmap(0,
               MAP_SIZE,
               PROT_READ | PROT_WRITE,
               MAP_SHARED,
               fd,
               0x40E00000 & ~MAP_MASK);
    if(map == (void*) -1) {
        perror("mmap()");
        exit(1);
    }
    // setting up the GPIO functions
gpio_function(DATA, GPIO);
gpio_function(CLK, GPIO);
gpio_function(CHIP_S, GPIO);
gpio_function(RESET, GPIO);
gpio_function(CH_A, GPIO);
gpio_function(CH_B, GPIO);
    // setting up the GPIO directions
    gpio_direction(DATA, OUT);
gpio_direction(CLK, OUT);
gpio_direction(CHIP_S, OUT);
gpio_direction(RESET, OUT);
gpio_direction(CH_A, OUT);
gpio_direction(CH_B, OUT);
    // start the RESET (and stay this way)
gpio_clear(RESET);
gpio_set(RESET);

// start reading file
static const char filename[]=“test_146.txt”;
FILE *file = fopen(filename,”r”);
if(file != NULL)
{
    char line [128]; // or other suitable maximum line size
    char addrBin[14] = “00000000000000”;    
    char valBin[8] = “00000000”;            
    int i = 0;
    int count198 = 0;

    // read a line
    while((fgets(line, sizeofline, file)!=NULL) && count198<198)
    {
        count198++; // ensuring the program
        char *pch;
        pch = strtok(line,”	”);
        int olddec,remain;
        int counter = 13;
        int address = atoi(pch);
        printf(“======the number is %d======
”,address);
        //converting decimal to 14-bit binary
        while(address>0)
        {
            olddec = address;
            remain = address % 2;
            address /= 2;
            if(remain == 1)
                addrBin[counter] = ‘1’;
            else
                addrBin[counter] = ‘0’;
            counter--;
        }
        pch = strtok(NULL, “	”);
        // converting hex to 8-bit binary
        if(pch[1] != NULL) {

The file read here is “test_146.txt” for channel 1, “text_223.txt” for channel 2, “text_467.txt” for channel 3, and “text_800.txt” for channel 4.
putBin(2,2,pch[0],valBin);
putBin(2,1,pch[1],valBin);
}
else {
    putBin(2,2,'0',valBin);
    putBin(2,1,pch[0],valBin);
}

// now we have the address and value

gpio_set(CHIPS);
gpio_clear(DATA);
gpio_clear(CLK);
gpio_clear(CHIPS);
gpio_clear(DATA);
gpio_clear(CLK);
gpio_set(CLK);
gpio_clear(CLK);

printf("====setting address======\n");
for(i=0; i<14; i++)
{
    if(addrBin[i] == '0') {
        printf("0");
        gpio_clear(DATA);
    }
    else {
        printf("1");
        gpio_set(DATA);
    }
    gpio_set(CLK);
    gpio_clear(CLK);
}
printf("\n");

gpio_clear(DATA);
gpio_set(CLK);
gpio_clear(CLK);

printf("====setting value======\n");
for(i=0; i<8; i++)
{
    if(valBin[i] == '0'){
        printf("0");
    }
}
gpio_clear(DATA);
}
else{
    printf("1");
    gpio_set(DATA);
}
}
gpio_set(CLK);
gpio_clear(CLK);
}
printf("\n");
gpio_set(CHIP_S);
}
fclose(file); // close the file

//=============end big loop (of 198 times)=================//

// Receive 1/2x mode initialization
printf("====normal address complete=========\n");
putBin(1,3,'0',addrBin);
putBin(1,2,'8',addrBin);
putBin(1,1,'C',addrBin);
putBin(2,2,'3',valBin);
putBin(2,1,'E',valBin);

gpio_set(CHIP_S);
gpio_clear(CHIP_S);
gpio_clear(DATA);
gpio_clear(CLK);
gpio_set(CLK);
gpio_clear(CLK);
printf("=====setting address======\n");
for(i=0; i<14; i++)
{
    if(addrBin[i] == '0') {
        printf("0");
        gpio_clear(DATA);
    }
    else {
        printf("1");
        gpio_set(DATA);
    }
}
```c
gpio_set(CLK);
gpio_clear(CLK);
}
printf("\n");

gpio_clear(DATA);
gpio_set(CLK);
gpio_clear(CLK);
printf("====setting value======\n");
for(i=0; i<8; i++)
{
    if(valBin[i] == '0') {
        printf("0");
        gpio_clear(DATA);
    }
    else {
        printf("1");
        gpio_set(DATA);
    }
    gpio_set(CLK);
gpio_clear(CLK);
}
printf("\n");

putBin(2,2,‘3’,valBin);
putBin(2,1,‘F’,valBin);

gpio_set(CHIPS);
gpio_clear(CHIPS);
gpio_clear(DATA);
gpio_clear(CLK);
gpio_set(CLK);
gpio_clear(CLK);
printf("====setting address======\n");
for(i=0; i<14; i++)
{
    if(addrBin[i] == ‘0’) {
        printf("0");
        gpio_clear(DATA);
    }
    ```
else {
    printf("1");
    gpio_set(DATA);
}
gpio_set(CLK);
gpio_clear(CLK);
}
printf("\n");

gpio_clear(DATA);
gpio_set(CLK);
gpio_clear(CLK);
printf("====setting value======\n");
for(i=0; i<8; i++)
{
    if(valBin[i] == ‘0’) {
        printf("0");
        gpio_clear(DATA);
    }
    else {
        printf("1");
        gpio_clear(DATA);
    }
    gpio_set(CLK);
gpio_clear(CLK);
}
printf("\n");
gpio_set(CHIPS);

// Transmit 1/2x mode initialization
putBin(1,3,’0’,addrBin);
putBin(1,2,’2’,addrBin);
putBin(1,1,’4’,addrBin);
putBin(2,2,’3’,valBin);
putBin(2,1,’E’,valBin);

gpio_set(CHIPS);
gpio_clear(CHIPS);
gpio_clear(DATA);
gpio_clear(CLK);

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gpio_set(CLK);
gpio_clear(CLK);

printf("====setting address=====
\n");
for(i=0; i<14; i++)
{
    if(addrBin[i] == '0') {
        printf("0");
        gpio_clear(DATA);
    }
    else {
        printf("1");
        gpio_set(DATA);
    }
    gpio_set(CLK);
gpio_clear(CLK);
}
printf("\n");
gpio_clear(DATA);
gpio_set(CLK);
gpio_clear(CLK);

printf("====setting value=====
\n");
for(i=0; i<8; i++)
{
    if(valBin[i] == '0')
    {
        printf("0");
        gpio_clear(DATA);
    }
    else
    {
        printf("1");
        gpio_set(DATA);
    }
    gpio_set(CLK);
gpio_clear(CLK);
}
printf("\n");
put Bin(2,2,'3',valBin);
putBin(2,1,'F',valBin);

gpio_set(CHIP_S);
gpio_clear(CHIP_S);
gpio_clear(DATA);
gpio_clear(CLK);
gpio_set(CLK);
gpio_clear(CLK);

printf("====Setting Address ======
");
for(i=0;i<14;i++)
{
    if(addrBin[i]=='0'){
        printf("0");
        gpio_clear(DATA);
    }
    else{
        printf("1");
        gpio_set(DATA);
    }
    gpio_set(CLK);
    gpio_clear(CLK);
}
printf("\n");
gpio_clear(DATA);
gpio_set(CLK);
gpio_clear(CLK);

printf("====Setting Value ======
");
for(i=0;i<8;i++)
{
    if(valBin[i]=='0'){
        printf("0");
        gpio_clear(DATA);
    }
    else{
        printf("1");
        gpio_set(DATA);
    }
    gpio_set(CLK);
    gpio_clear(CLK);
}
printf("\n");
gpio_set(CHIP_S);

    // sending channel information
    gpio_clear(CH_A);\(^{12}\)
    gpio_clear(CH_B);\(^{13}\)
}
else{
    printf("file does not exist");
    printf("\n");
}
return 0;
}

A.2 Python Program

/**************************************************************/
/* Copyright ©April, 2008 Rithirong Thandee <rthandee@vt.edu>*/
/**************************************************************/
#!/usr/bin/env python

import pygtk
pygtk.require('2.0')
import gtk
import os, sys, string

#-----------------------------------------------------------
# Memory Location Definitions
# Refer to Inter® PXA270 Processor Developer’s Manual
#-----------------------------------------------------------
GPIO_BASE_OFFSET = 0x40E00000
SPIDirROff = 0x00000014

\(^{12}\)Use this command for channels 1 and 2, and use the command “gpio_set(CH_A);” for channels 3 and 4.

\(^{13}\)Use this command for channels 1 and 3, and use the command “gpio_set(CH_B);” for channels 2 and 4.
SPIAROff = 0x00000068

# Register definitions in byte locations
NSSPCR0_BL = 0x41400000
NSSPCR1_BL = 0x00000004
NSSSR_BL = 0x00000008
NSSITR_BL = 0x0000000C
NSSDR_BL = 0x00000010
NSST0_BL = 0x00000028
NSSPSP_BL = 0x0000002C

# Register definitions in word locations
NSSPCR0 = 0x41400000
NSSPCR1 = 0x00000001
NSSSR = 0x00000002
NSSITR = 0x00000003
NSSDR = 0x00000004
NSST0 = 0x0000000a
NSSPSP = 0x0000000b

class Demo04:

def Denary2Binary(self, n):
    """convert denary (base 10) integer n to binary string bStr""
    bStr = ''
    if n<0: raise ValueError, "must be a positive"
    if n==0: return '0'
    while n>0:
        bStr = str(n % 2) + bStr
        n = n >> 1
    return bStr

def sendData(self, data):
    #getting the data from the callback function
    #myfile will import the data file
    if data == 146:
        os.system("./spi_read_146")
    elif data = 223.5:
        os.system("./spi_read_223.5")
    elif data = 467:
        os.system("./spi_read_467")
    elif data == 800:
        os.system("./spi_read_800")
#function callback to get one thing done anymore

def callback(self, widget, data):
    if data == "146.5MHz":
        self.sendData(146.5)
    elif data == "223.5":
        self.sendData(223.5)
    elif data == "467":
        self.sendData(467)
    elif data == "800":
        self.sendData(800)


def delete_event(self, widget, event, data=None):
    gtk.main_quit()
    return False

#-----------------------------------------------------------
# These functions are straightly from the pygtk tutorial
# and almost self explainatory
#-----------------------------------------------------------

def init_(self):
    self.window = gtk.Window(gtk.WINDOW_TOPLEVEL)
    self.window.set_size_request(480,272)
    self.window.set_title("VT Public Safety Radio")
    self.window.connect("delete_event",self.delete_event)
    self.window.set_border_width(10)

    self.image4 = gtk.Image()
    self.image4.set_from_file("banner.gif")
    self.myHBox = gtk.HBox(False, 0)
    self.myVBox = gtk.VBox(False, 0)
    self.window.add(self.myVBoxAll)
    self.myVBoxAll.pack_start(self.imag4,False,False,0)
    self.image4.show()
    self.myVBoxAll.pack_start(self.myHBox)

    self.button1 = gtk.Button("146.5MHz")
    self.button1.modify_bg(gtk.STATE_NORMAL,gtk.gdk.color_parse("#962A1C"))
    self.button1.connect("pressed",self.callback,"146")
    self.myHBox.pack_start(self.button1,True,True,0)
    self.button1.show()
self.button2 = gtk.Button("223.5MHz")
self.button2.modify_bg(gtk.STATE_NORMAL,gtk.gdk.color_parse("#228b22"))
self.button2.connect("pressed",self.callback,"223.5")
self.myHBox.pack_start(self.button2,True,True,0)
self.button2.show()

self.button3 = gtk.Button("467.6125MHz")
self.button3.modify_bg(gtk.STATE_NORMAL,gtk.gdk.color_parse("#ffa500"))
self.button3.connect("pressed",self.callback,"467")
self.myHBox.pack_start(self.button3,True,True,0)
self.button3.show()

self.button4 = gtk.Button("800MHz")
self.button4.modify_bg(gtk.STATE_NORMAL,gtk.gdk.color_parse("#b03060"))
self.button4.connect("pressed",self.callback,"800")
self.myHBox.pack_start(self.button4,True,True,0)
self.button4.show()

self.myHBox.show()
self.myVBoxAll.show()
self.window.show()

def main():
    gtk.main()

if __name__ == "__main__":
    hello = Demo04()
    main()

B Troubleshooting Resources

Website: http://www.gumstix.com/support.html
Mailing List: gumstix-users@lists.sourceforge.net
IRC’s channel: #gumstix