Investigation of a Negative Impedance Converter for Wide Band Antenna Matching

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# Table of Contents

1 Introduction .......................................................................................................................... 3  
2 Circuit Description .............................................................................................................. 3  
3 PSPICE Simulation ............................................................................................................. 4  
4 Testing and Measured Results ............................................................................................ 7  
5 Layout Details ..................................................................................................................... 12  
6 Summary ................................................................................................................................ 17  
Appendix 1: Parts List ............................................................................................................ 18  
Appendix 2: PSPICE Listing .................................................................................................. 21  
References .................................................................................................................................. 22
1 Introduction

A simple monopole antenna such as is often used in a mobile radio installation is typically designed to operate in a resonant mode. Resonance is defined as the frequency where the antenna terminal impedance is purely resistive (having a zero reactive component). Although exact resonance only occurs at a single frequency, the antenna will have some bandwidth where the reactive component of the impedance is small. The resistance presented at the monopole antenna terminals is primarily radiation resistance. Radiation resistance is due to energy that is actually radiated from the antenna. When receiving, radiation resistance is the impedance of the antenna, as a source.

It is desirable to operate over some range of frequencies. As the operating frequency moves away from resonance the radiation resistance changes gradually but the reactance changes fairly rapidly. At some point the impedance gets far enough from the nominal value to cause significant signal loss. Circuit theory provides no fixed network of passive components that will completely compensate for the mismatch at the antenna terminals over a wide band of frequencies. The goal of Non-Foster Matching is to compensate for the mismatch by canceling the reactance at the antenna terminal with a reactance having the opposite sign but the same frequency dependence. Non-Foster matching requires the use of some combination of components including a negative capacitor or negative inductor. These non-Foster elements are only produced artificially with active (e.g. transistor) circuits. Such a circuit is known as a Negative Impedance Converter (NIC). A plan for implementing a NIC as part of antenna system is outlined in a report by Ellingson [1].

This study attempts to implement a negative capacitor. A negative capacitor has the same magnitude of reactance but the opposite sign as the reactance of the corresponding capacitor. The reactance of a capacitor has a negative sign. The reactance of a negative capacitor will, therefore, have a positive sign. That means that the negative capacitor appears to be an inductor when evaluated at a single frequency. The frequency dependence of a negative capacitor is the inverse of the inductor, however [2].

The Negative Impedance Converter was implemented and shown to produce a reactance that canceled the reactance of a fixed capacitor in both a series and shunt configuration. Direct measurements of the NIC input impedance were made using a Vector Network Analyzer (VNA). VNA measurements demonstrated that the NIC could produce a reactance having the same sign as a negative capacitor (or an inductor). The anticipated frequency dependence of a non-Foster reactance was not demonstrated, however.

2 Circuit Description

The NIC tests were performed on a Linville OCS (Open Circuit Stable) design presented by Sussman-Fort and Rudish [3]. Their circuit was provided with component values. No layout or component list was
provided, however. The goal of this study was to reproduce it as closely as possible and study its characteristics.

This particular Linville OCS NIC is a two port feedback device. It is normally operated in a shunt mode where one port presents the non-Foster impedance while the other port connects to an ordinary impedance that is to be transformed to a non-Foster impedance. The first port presents the non-Foster impedance (in shunt) with respect to ground. Shunt mode operation limits the utility of the circuit to cases where either the NIC is in parallel with the remaining circuit or where the remaining circuit is floating with respect to ground.

Since the circuit is “open circuit stable”, it tends to be stable when the impedance at the terminals combined with the impedance of the NIC is high. If the impedance is low the circuit may oscillate.

The ideal Linville OCS NIC is expected to produce a capacitance of \( C_{in} = -\frac{R_1}{R_2}C_L \). The actual value will vary somewhat due to variations in real components as well as the bias and compensation components required for the real design [3].

![Figure 1: NIC Circuit of Sussman-Fort and Rudish.](image)

### 3 PSPICE Simulation

The NIC circuit (fig. 1) was simulated in PSPICE circuit simulation software. The initial simulations were performed with all components at the values provided by Sussman-Fort and Rudish [3]. The initial value
of C2 was 47pF. All passive components were treated as ideal devices. The transistors were modeled as real devices, however. The circuit was found to be stable in simulation under several load conditions including direct connection, series and parallel capacitance (figs. 3A, 3B and 3D).

The final simulation was done with C2 having a 4700pF (4.7nF) value after that was found to be more stable in practice. A series capacitance simulation was tested using values of $C_L=47pF$ and $C=60pF$. The results were plotted separately as magnitude of Z and phase (fig. 2). The plots display a resonance at about 30 MHz. This is similar to the measured result shown below in figures 4 and 5.

![Figure 2: PSPICE Simulation of NIC with $C_L=47pF$ and $C=60pF$ Series Capacitance.](image_url)
Figure 3: NIC Test Cases

A. Direct Connection to VNA Port

B. Parallel C

C. Series R C

D. Series C

E. Series R
4 Testing and Measured Results

A NIC printed circuit board was produced and populated for testing. The circuit closely followed the Sussman-Fort design. Some changes were made at C1, C2 and C10. A detailed schematic is shown below in figure 10.

The NIC was tested in several configurations as shown in Figure 3. \( Z_{\text{vna}} \) represents the Vector Network Analyzer (VNA) with its 50 Ohm port impedance. \( C_L \) is the load impedance to be negated by the NIC. The NIC circuit is the Linville OCS design of Sussman-Fort and Rudish. \( C \) is the test reactance. Also, when testing for oscillations, \( Z_{\text{vna}} \) represents a 50 Ohm spectrum analyzer port.

The direct connection (fig. 3A) oscillates strongly at low frequency (about 89 kHz) with the current component values and was not measured for operation as a NIC. The oscillation frequency is somewhat dependent on the values chosen for the bias inductors. The parallel capacitor case (fig. 3B) also oscillates. Since the circuit is “open circuit stable” the parallel capacitor case would seem to be a good choice. In our test circuit, however, the parallel 50 Ohm resistance of the network analyzer port dominates the port impedance at low frequencies resulting in an unstable case. The direct and parallel capacitor cases were not considered further.

Another important consideration is the power level of the RF test signals. The Vector Network Analyzer (VNA) is capable of exciting the test circuit with a signal level of up to 1 mW (0 dBm). That level causes compression in the circuit. -30 dBm is used in the measurements in order to ensure that small signal conditions are satisfied for the transistors. Some of the plots appear noisy due to the relatively low excitation level.
The series connected case (fig. 3C) provides for cancellation of the reactance of C by the negative capacitance of the NIC. In order to achieve a high degree of cancellation it is necessary to carefully adjust the value of the C (or C_L). The cancellation is observed in figures 4 and 5 for values of C_L=47pF and C ~ 60pF. C is carefully adjusted with a trimmer capacitor to achieve the smallest magnitude Z. This measurement may be compared with the simulation (fig. 2) which has some corresponding features. There are several interesting differences between the simulation and the realized circuit operation, however. The differences are attributed to a combination of non-ideal components and measurement setup.

Figure 4: Measured Magnitude Z of NIC with C_L=47pF, Series C=60pF (approximate).
It is expected that a series capacitance circuit (fig. 3D) at the NIC OCS port can cause instability when the test capacitance \( C \) is similar in value to the calculated NIC input negative capacitance \( C_{in} \). This is expected since, in the series connection, a low impedance is seen by the NIC due to the cancellation of the positive capacitance by the negative capacitance generated in the NIC. This OCS (open circuit stable) NIC design is most stable when terminated in a high impedance condition (including the negative capacitance of the NIC itself). This effect was observed at a single frequency in figure 5 at marker 3 where there are spikes in the phase occur at the onset of instability. In real time the spikes were observed to vary while the corresponding point in figure 4 was found to go slightly negative. The advantage in the series connection is that a high capacitive reactance is presented to the NIC at low frequencies where (in this circuit) the potential for oscillation is higher than it is at higher frequencies.
The series connected capacitor, series resistor case (fig. 3C) was tested using $C = 68\,\text{pF}$ and $R = 51\,\text{Ohms}$. $C_L$ remained the same at $47\,\text{pF}$. Measured results were presented in Smith Chart format in figure 6. Perfect cancellation of the reactive components occurred at approximately $50\,\text{MHz}$. The same data was plotted in figure 7 as VSWR. All of the markers ($40$ to $70\,\text{MHz}$) fell within the VSWR value of $2$. With $Z_{in}=50\,\text{Ohms}$ this circuit was expected to have a very low $Q$. An ordinary series RLC circuit had almost the same response.

In order to make a more direct test while avoiding oscillations due to low impedance termination of the OCS port a series resistor $R$ (Fig. 3E) was inserted between the NIC and VNA. A resistor value of $100\,\text{Ohms}$ was found to be sufficient to ensure stability. In order to find the actual NIC port impedance, the $100\,\text{Ohm}$ resistance was extracted from the measured results using “trace math” function of the VNA. The display then shows the de-embedded NIC port impedance. Figure 8 shows the impedance of the NIC over the frequency range of $10$ to $110\,\text{MHz}$. The result appears inductive over this entire range. Reactance increases over the frequency range from low frequency to high. This is similar to the response.

Figure 6: Measured Smith Chart of NIC with $C_L=47\,\text{pF}$, Series $C=68\,\text{pF}$ and $R=51\,\text{Ohms}$. 

![Smith Chart Image]
expected from an inductor. A negative capacitor is expected to decrease in reactance as the frequency is increased [4].

![Graph showing VSWR plot]

Figure 7: Measured VSWR Plot of NIC with \( C_L = 47 \text{pF} \), Series \( C = 68 \text{pF} + R = 51 \text{Ohms} \).
A further test was performed to ensure that the modified value of C3 did not cause improper operation of the NIC circuit. The original value of 47pF was restored to the circuit at C3. The previous test was repeated using the same 100 Ohm series resistor configured as in figure 3E. The circuit was found to be stable with the higher port impedance. While the impedance (fig. 8) changed significantly at low frequencies, only a relatively small shift in impedance was observed in the range of 50 to 110 MHz. No part of the frequency range seems to correspond to a non-Foster element, however.
Figure 9: De-embedded input impedance of NIC tested with Series $R=100$ Ohms, $C_L=47\text{pF}$ and $C_3$ restored to original $47\text{pF}$. 
5 Layout Details

The board layout is a two layer design with a (almost) complete ground plane as one layer. Most passive components are 0602 (inch unit). The transistors are also surface mount. Through hole footprints were chosen for the Voltage regulator as well as the RF and header strip connections for the sake of ruggedness. The layout was a compromise between the requirements for small size and ease of hand assembly.

A number of spare footprints were provided at each port of the NIC to facilitate the introduction of complex impedances for operational and testing purposes. Footprints at the ports were used to insert resistors and capacitors as needed for the test configurations.

For the purposes of initial testing SMA connectors were attached to each port. The voltage regulator was omitted and a regulated bench supply was used. Ferrite beads on the layout were solder-bridged.

A circuit board schematic is shown in figure 10. A photograph of the circuit board is shown in figure 11. Figure 12 shows details of the circuit board layout. The reverse of the circuit board is a complete ground plane with the exception of one small break for a crossover and the mounting holes. Solder mask is provided on both front and back of the board. A detailed parts list is contained in Appendix 1.
Figure 10: Circuit Board Schematic.
Figure 11: Photograph of Test Circuit Board
6 Summary

A NIC was implemented and tested to determine if a non-Foster capacitance could be produced. Circuit stability was an important issue with the circuit. The NIC tended to break into oscillation under some load impedance conditions. An important stability case was when the NIC was presented with a relatively low impedance of 50 Ohms at the input port. The typical 50 Ohm radio antenna port connected to the NIC, in some configurations, caused instability in this circuit. Higher port impedances of 150 Ohms or more were found to be adequate to prevent oscillation under most conditions.

The NIC was expected to produce a non-Foster impedance at the input port of the circuit. This did not appear to be the case with this implementation. Measurements of the NIC circuit using both series and parallel capacitors demonstrated resonant effects. Direct VNA measurements showed that the NIC produced a reactance having the expected sign but with the frequency dependence of an inductor. The
The circuit appeared to behave largely as a low-Q inductor over the frequency range tested. The low-Q inductance produced by the NIC was found to be useful for operation in the range of 30 to 110 MHz.

An analytical investigation is recommended to understand why the NIC did not work entirely as expected. It is unclear if test conditions may have caused the discrepancy. It is possible that non-Foster results may be obtained with this circuit in some configuration other than attempted here. It is also likely that non-Foster effects were produced but masked by undesired reactances in the circuit.

Circuit implementation issues should be given more consideration. The bias inductors used at L2 and L7 have lower self-resonant frequencies than desired. Better inductors could have improved circuit operation. The effects of compensation components R3, C1 and C10 need more study. R3 and C1 are specified as “tunable”. The procedure for determining the best values of these components is not entirely clear. The “parasitic modeling” capacitor at C10 has a large effect on circuit operation. The correct value is difficult to determine empirically. The value used at C10 was chosen for best match with the PSPICE simulation. There is some variation with temperature that makes the best operation difficult to maintain. Improved biasing may improve temperature stability.

A final concern is the 50 Ohm port impedance of the Vector Network Analyzer used as a measurement device. The feedback conditions of the NIC are likely to be affected by the impedance seen at the NIC terminals. It is possible that 50 Ohm impedance is inappropriate for proper operation of the NIC in the configurations used for this work. A high impedance may be more appropriate for testing in the shunt C configuration for instance.

### Appendix 1: Parts List

<table>
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<th>Schematic Ref.</th>
<th>Nominal Value</th>
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Appendix 2: PSPICE Listing

* EESchema Netlist Version 1.1 (Spice format) creation date: 5/31/2012 10:27:56 PM

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Q1 5 7 8 NE85600
CCB 7 5 0.09E-12
CCE 5 8 0.16E-12
LE 8 6 0.93E-9
LB 4 7 1.4E-9
CCPKG 4 5 0.12E-12
CCEPKG 5 6 0.16E-12
CBPKG 4 6 0.04E-12
LBX 1 4 0.2E-9
LCX 5 2 0.2E-9
LEX 6 3 0.2E-9

.MODEL NE85600 NPN
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+ ISE=32e-16 NE=1.93 BR=12 NR=0.991 VAR=3.9
+ IKR=0.17 ISC=0 NC=2 RE=0.38 RB=4.16
+ RBM=3.6 IRB=1.96e-4 RC=2 CJE=2.8e-12 VJE=1.3
+ MJE=0.5 CJC=1.1e-12 VJC=0.7 MJC=0.55 XCJC=0.3
+ CJS=0 VJS=0.75 MJS=0 FC=0.5 TF=10e-12
+ XTF=6 VTF=10 ITF=0.2 PTF=0 TR=1e-9
+ EG=1.11 XTB=0 XTI=3 KF=1.56e-18 AF=1.49 )

.ENDS

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V1 30 0 AC .0001
Vin 1 0 DC 20
*R99 31 30 50
R99 14 30 50
*C98 31 14 58pF
C99 14 0 58pF
R98 14 0 100G
R1 3 0 110
R6 2 3 47
C1 3 0 12.75pF
L1 3 2 8nH
L3  5 8 22nH
XQ2  9 5 2 NE85630/CEL
R12  1 9 1500
L7  15 1 10uH
XQ1  6 16 10 NE85630/CEL
CL1  8 0 47pF
*CL1  8 31 .1uF
*RL1  31 0 100
C6  9 4 .0047uF
C2  8 6 47pF
C10  4 0 4.7pF
C5  16 4 .0047uF
C8  10 11 .0047uF
C3  14 10 .0047uF
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R4  6 15 750
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References