Announcement

• Pick a partner for project 5 by Tuesday.
  – Send me e-mail with both partners names by Tuesday at 5 p.m. (from one person only please)
  – If I don't receive an e-mail, I'll assign you a partner.

Last time

• More synthesis examples:
  – Sensitivity lists
  – Variable/signal assignment
  – Rules for generating sequential logic
  – Combinational hardware examples

Xilinx FPGAs

XC2S100

Field Programmable Gate Arrays
(Chip function controlled by SRAM control bits)

ASICS vs FPGAs

• FPGA advantages
  – Lower initial cost
  – Faster development cycles
  – Lower risk
  – Design upgrades in the field with no hardware replacement.
  – Easier to test

• ASIC advantages
  – Higher speed
  – Lower cost in large volumes

Spartan 2 Family Features (1/3)

• Unlimited Reprogrammability
• S-Ram programming technology
• Volatile
• Musts be re-programmed on power up
• High speed carry logic
• Dedicated multiplier support
• Cascade chain for wide input functions
• Internal 3-state bus capability
Spartan 2 Family Features (2/3)

- Registers/Latches with enable, set, reset
- Four dedicated DLLs
  - Delay Locked Loops
- Four primary low-skew global clock nets
- IEEE 1149.1 compatible boundary scan logic
- SelectRAM hierarchical memory
  - 16-bit LUT based distributed RAM
  - Configurable 4K-bit block RAM
  - Fast interfaces to external RAM

Spartan 2 Family I/O Features (3/3)

- Fully PCI compliant
- 16 High Performance Interface Standards
- Zero hold-time

Spartan 2 Family Block Diagram

XC2S100 Parameters

- 2,700 Logic Cells
- 100,000 equivalent gates
- 20x30 CLB array
- 196 user I/O
- 38,400 distributed RAM bits
- 40K block RAM bits

Programming FPGAs

- Load configuration data into internal RAM memory cells.
  - On power up, actively read configuration data from an external PROM
    - XSA board uses FLASH memory
  - Configuration data written into the FPGA under control of an external device (programmer)
    - XSA board uses
      - CPLD chip and PC parallel port
      - GXSLOAD program

Three Important Programmable Logical Elements

a) Lookup Table (LUT)
b) Programmable Interconnection Point (PIP)
c) Control MUX
Programming of the simple CLB to implement a JK flip-flop

Look Up Table
Contents for JK

Uses of LUTs in a Logic Cell
- Implement any 4-input, 1-output combinational logic function
- Implement a 16x1 synchronous RAM
- Implement a 16-bit shift register
FFs in a Slice

- Share common
  - Clock signal
  - Clock signal enable
  - Set signal
  - Reset signal
- Must both be configured to be (have)
  - Edge-triggered D Flip-Flops
  - Level-sensitive latches
  - Synchronous set and/or synchronous reset
  - Asynchronous set and/or asynchronous reset
- All control signals are independently invertible

RAM in a Slice

- The two LUTs in a slice can be configured to implement
  - 16x2 Synchronous RAM
  - 32x1 Synchronous RAM
  - 16x1 Dual Port Synchronous RAM

Combinational Logic in a Slice

- Any function of 5 variables
- A 4X1 Multiplexer
- Selected functions of up to 9 variables

Slice Logic Configured to Implement any Function of 5 Variables

- A LUT with inputs A, B, C, D, E and outputs F(A, B, C, D, 0) and F(A, B, C, D, 1)
Configurable Logic Block (CLB)

XC2S100 chip has 20x30 Array of CLBs

CLB Logic

CLB Logic Configurations

- Implement any function of 6 input variables
- Implement an 8x1 multiplexer
- Implement selected functions of up to 19 input variables

Exercise for the reader:
Show how to configure the CLB to implement any function of 6 variables.

Arithmetic Functions

- Each CLB supports two separate carry chains, one per slice. The height of each carry chain is two bits per CLB.
- An XOR gate allows a 1-bit full adder to be implemented in each Logic Cell
- A dedicated AND gate improves the efficiency of multiplier implementation

Block RAMs on XC2S100 Chip

XC2S100 chip has 10 4K Blocks

4K Dual Port Block RAMs
**DLL Circuits**

- Eliminate skew between the clock input pad and internal clock-distribution-nets
- Advanced control of multiple clocks
  - Provides four quadrature phases of source clock
  - Can double the rate of the source clock
  - Divide source clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16
- Deskew a board clock
  - Clock an external device from an FPGA pin
  - Read the external clock back in on another pin
  - Use a DLL circuit to synchronize the two clocks

**Programmable Routing Matrix**

- Principle
  - The longest delay path limits the speed of any design.
- Xilinx Claim
  - Spartan 2 routing architecture and the place and route software were developed together to provide optimization advantages.

**Local Routing**

**General Purpose Routing Resources**

- Each CLB has a GRM (General Routing Matrix)
  - Connects horizontal and vertical routing resources
  - Connects its CLB to the routing matrix
- 24 single length lines connect adjacent GRMs in each of four directions
- 96 buffered HEX lines connect each GRM to other GRMs six blocks away in each of four directions
  - Staggered pattern
  - Driven only at end points
  - Accessed at end points and at mid points
  - 1/3 are bidirectional
- 12 buffered bi-directional long lines

**Global Routing**

- Primary Global Routing
  - 4 Dedicated global nets with dedicated input pins to distribute high-fanout clock signals with minimum skew
  - Each can drive ALL CLBs, IOBs, and Block RAMS
  - Each has its own dedicated global buffer driver
- Secondary Global Routing
  - Up to 12 unique signals per column can be distributed on the 12 long lines dedicated to each column
  - May be driven from internal CLBs

**Clock Distribution**

- [Diagram of clock distribution]
Dedicated Routing

- I/O Routing
  - VersaRing
  - Connect GRM array to I/O Blocks
- Horizontal 3-state busses
- Vertical carry signal propagation between adjacent CLBs

Tri-state Busses

Input/Output Block (IOB)

IOB Registers

- Configurations
  - Edge-triggered Flip Flops
  - Level-sensitive latches
- Common clock for all IOB FFs
- Independent enable for each IOB FF
- Common set/reset signal for all three IOB FFs independently programmable for each FF
  - Synchronous or asynchronous set
  - Synchronous or asynchronous reset
- IOB buffers and all control signals may be independently programmed to be active-high or active-low

Standards Supported

I/O Pads

- Optional pull-up resistors
- Optional pull-down resistors
- Optional weak-keeper circuits
XC2S100 Chip has only 4 banks.

Summary

- Features of FPGAs in general and the Xilinx Spartan II in particular
  - CLB
  - Programmable interconnect

- Next time: Go over project 5 and the class hardware.