Introduction and Motivation

Designing Large Systems

- Can design modest systems using techniques learned in ECE 3504.
- How do you design a 100 million gate design?
  - Without errors?
  - In 18 - 24 months?

Designing Hardware

- How does one design:
  - Large Digital Systems?
  - Specialized applications?
  - Computer boards?
  - Computer processors?
- How do design teams in an organization exchange information?

Classical Design Process

- Written Specification
- State Diagram
- State Table
- State Assignment
- Kmaps - Quine McCluskey
- Circuit Diagram
- Simulate Circuit (LogicWorks)

Deficiencies of Classical Design Process

- Difficult to specify the system in an unambiguous manner.
- Design cannot be checked until the last step.
- Acceptance testing: How do you know the delivered product meets specifications?

Why VHDL Was Created

- To provide unambiguous executable specification (Behavioral Model)
- To support design decomposition (Structural Model)
- To support mixed level simulation
- To support acceptance testing.
Advantages of Hardware Description Languages

- Can model, simulate, and validate designs without the construction of expensive hardware prototypes.
- Able to exchange hardware models with other teams in overall design effort without compromising design secrets.
- Able to use different levels of abstraction in design process.
- Allows reuse of previously designed material.

VHDL - the acronyms

- VHDL
  - VHSIC Hardware Description Language
- VHSIC
  - Very High Speed Integrated Circuit

What is VHDL?

A Simulation Modeling Language

- VHDL has many features appropriate for describing the behavior of electronic components:
  - Simple logic gates to complete microprocessors.
- VHDL simulation models can then be used as building blocks in larger circuits (using schematics, block diagrams or system-level VHDL descriptions) for the purpose of simulation.

What is VHDL?

A Design Entry Language

- VHDL allows the behavior of complex electronic circuits to be captured into a design system for automatic circuit synthesis.
- Used for the synthesis of everything from PLDs to ASICs.

What is VHDL?

A Test Language

- One of the most important aspects of VHDL is its ability to capture the performance specification for a circuit, in a form commonly referred to as a test bench. Test benches are VHDL descriptions of circuit stimulus and corresponding expected outputs that verify the behavior of a circuit over time.

What is VHDL?

A Netlist Language

- Useful as a low-level form of communication between different tools in a computer-based design environment.
- VHDL’s structural language features allow it to be effectively used as a netlist language, replacing other netlist languages such as EDIF.
What is VHDL?

A Standard Language

- VHDL is a standard in the electronic design community.
- Using a standard language such as VHDL will virtually guarantee that you will not have to throw away and re-capture design concepts.

Other Hardware Description Languages

- VHDL (IEEE Standard 1076B)
- Verilog
- UDL/I
- ABEL
- IHDL (Intel's Hardware Description Language)

Some VHDL Basics...

- VHDL allows one to model systems where more than one thing is going on at a time
  - Concurrency
  - Discrete event simulation

Basics (cont'd)

- VHDL allows modeling to occur at more than one level of abstraction
  - behavioral
  - register transfer
  - Boolean equation
  - gates

Why is this important?

- Formal specification
- Testing & validation w/ simulation
- Performance prediction
- Automatic synthesis
- Top-down modeling
  - Behav → RTL → Boolean → Gates → Transistors

HDLs vs. Software

- Similar in that:
  - task described by structured code
  - sub-modules procedures, functions
  - portable
- Different in that:
  - timing information implied in software
  - all timing explicit in HDLs
Motivation for HDL's:
- Create the correct design on time

Reading for next time:
- Chapters 1 and 2.
- We'll talk about the design process