ECE 4514 Digital Design II
Project 2

Assigned: September 16, 2003
Due: September 30, 2003, beginning of class.
This assignment is to be completed individually.

Create a VHDL model for a 3-bit counter that can count up or down in either binary or Gray code. The counter has 4 inputs, clock, reset, mode, and up_down, and a 3-bit output, count. Reset is asynchronous and active low, i.e. when reset = 0, the counter output is 000, and when reset = 1, the counter is active. When the counter is active, the output changes on the falling edge of clock. When the output changes, its new value depends upon the values of mode and up_down.

When mode = 1 and up_down = 1, the counter goes through the sequence 000, 001, 010, 011, 100, 101, 110, 111, and then repeats. When mode = 0 and up_down = 1, the counter goes through the Gray code sequence 000, 100, 101, 001, 011, 111, 110, 010, and then repeats. When up_down = 0 in either mode, the sequence is reversed for that mode. When mode changes, the outputs of the counter on the following clock edges should be the proper ones for the new value of mode. For example, if the current value of count is 111, up_down = 1, and mode changes from 1 to 0, then the next value of count will be 110, followed by 010, and so on.

Use exactly the following entity declaration for your counter:

ENTITY gray_bin_counter IS
  PORT (
    clock, reset, mode, up_down: in bit;
    count: out bit_vector(2 downto 0)
  );
END gray_bin_counter;

Your model should not use any delays, i.e. there should not be any “after” clauses on any of the assignments.

Create a testbench to simulate your counter sufficiently to verify the functionality, and include the simulation results in your report. Include a hardcopy of your counter model and your testbench in your report.

The name of your architecture for the gray_bin_counter entity should be your PID, and the name of the file should be gray_bin_counter_<insert your PID>.vhd. (E.g., for me, the architecture would be named tlmartin and my file would be named gray_bin_counter_tlmartin.vhd.) Your code should be appropriately commented and ready to be analyzed. Before class on the due date, e-mail your VHDL model of the counter (not your testbench) as an attachment to our TA, Ed Curley, at curley@vt.edu. He will use a testbench to verify that your model meets the above specifications.

Report format and credit: (100 points maximum)

Note: In addition to items listed here, your report must conform to the specifications provided in the class syllabus. Submission of a disk is not required, however.

- Signed cover sheet (5 points)
- Descriptive documentation as per syllabus (15 points)
- Commented architecture for binary/Gray code counter (printed and attached) (10 points)
- Testbench (printed and attached) (10 points)
- Simulation results demonstrating that model meets all specifications (25 points)
- Emailed binary/Gray architecture (properly named and analyzable) (5 points)
- Conformance to secret testbench results (30 points)
Abstract: A binary/Gray code counter is modeled. The counter meets the specifications provided in the project description.

Honor Code:

I pledge that this is my own work and I have neither copied it from a colleague nor given it to an associate.

Signed: __________________________________________