Figure 1. NCDesktop Window

Figure 2. Opening window properly filled in.
Figure 3. The main window.
Figure 4. Entity “clk” is now added to the working library.
Figure 5. Modules “clk” and “clk_testbench” have now been analyzed.
Figure 6. Elaborate the top level construct, highlighted above.
Figure 7. Results of elaboration.
Figure 8. The simulator window.

```vhdl
architecture CLK_TEST of CLK_TESTBENCH is
    -- Declare the component to be tested
    component CLK
        generic (PERIOD : TIME := 100 ns);
        port (ENABLE : in BIT := '0';
            CLK_OUT : out BIT := '0');
    end component;

    -- Declare internal testbench signals
    signal TB_ENABLE1, TB_ENABLE2 : Bit := '0';
    signal TB_CLK1, TB_CLK2 : Bit := '0';
    for all : CLK use entity work.CK(BHV);
begin
```

Figure 9. The Watch window.
Figure 10. The waveform display window.
Figure 11. Breakpoint screen.
Figure 12. Simulation of the clock module.
Figure 13. Cursors positioned to measure the period of a clock wave.
Figure 14. The Navigator window
Figure 15. The expanded model in the left-hand section.
Figure 16. Module C1 selected, variable COUNT selected
Figure 17. Add a variable to the display.