A 100 MHz – 2.5 GHz Direct Conversion CMOS Transceiver for SDR Applications

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Abstract — This paper describes a fundamentally flexible low power transceiver implemented in 90 nm CMOS. Novel circuit architectures have been implemented to overcome problems that have encumbered wideband transceivers in the past. Flexible programming allows the RFIC to process signals of multiple wireless protocols from 100 MHz – 2.5 GHz with channel bandwidths from 8 KHz to 20 MHz. At 1.8 GHz the receiver noise figure is 7 dB with IP3 of –6 dBm and voltage gain of 48 dB. The transmitter has better than 40 dB carrier suppression, 35 dB sideband suppression, and EVM of 1% at 800 MHz. The frequency synthesizer uses direct digital synthesis to achieve instantaneous frequency switching and phase noise of –123 dBc/Hz at 25 KHz offset.

Index Terms — CMOS, Direct Conversion, DDS, SDR, Transceiver

I. INTRODUCTION

The benefits of software defined radio (SDR) have been known for years [1]. For military and public safety applications SDR promises interoperability. For the makers of consumer communications products, SDR will enable faster time to market and the ability to use a common radio platform across product lines. Above all, SDR will be a key enabler of cognitive radio [2], where a device can sense and adapt to its spectral environment, for example by using unoccupied TV bands [3].

Despite intense interest in realizing these benefits, few SDR-enabling integrated transceivers have been reported to date [4].

Challenges in implementing SDR stem from its broadband nature. Receiver architectures must be chosen that minimize the need for filtering since low-loss, broadband tunable filters are not practical in today’s technology [5]-[7]. Direct conversion is preferred for this reason, but it has some disadvantages that must be addressed through circuit techniques as discussed in Section II. Quadrature Local Oscillator (LO) generation over a wide frequency range is another challenge that is typically addressed with multiple high frequency VCOs and complex divider schemes [8]. Unfortunately, this approach often leads to spot coverage that targets some subset of predefined frequencies. Direct digital synthesis offers some attractive features like fast switching and continuous coverage, but again, it has disadvantages that require particular attention. Our solutions to these challenges and others will be discussed in Section II.

II. ARCHITECTURE

Referring to Fig. 1, three independent direct digital synthesizers (DDS) use a single 1 GHz PLL reference to provide differential quadrature LO signals to the receiver, transmitter, and Cartesian feedback mixers. Direct conversion is used in the receiver and a direct launch quadrature modulator is used in the transmitter. One of five receiver paths is selected to drive a common analog baseband low pass filter section with programmable corner from 4 KHz to 10 MHz. There are provisions for receiver Automatic Gain Control (AGC), DC offset correction, and in band and out of band Receiver Signal Strength Indicator (RSSI). Dynamic matching is used in the direct conversion mixers for improved second order intermodulation intercept point (IP2), flicker noise, and DC offset. Differential baseband analog in-phase and quadrature receiver signal outputs are provided for external connection to an ADC and digital processing.
Differential baseband in-phase and quadrature inputs from an external transmitter DAC are applied to programmable low pass filters similar to the receiver with 10% bandwidth steps from 4 KHz to 10 MHz bandwidth. There is one of three selectable transmitter paths with up to 90 dB of on chip programmable gain available (for power control). A transmitter feedback network is provided for closed loop narrow band linearization or open loop alternative transmit signal analysis and processing.

A. Receiver

The RFIC contains 5 fully differential receiver inputs that drive fully differential, dynamically matched (chopping), passive, quadrature (I/Q) mixers. Four of the receiver inputs each include an LNA. Baseband filters that support multiple bandwidths are also implemented along with gain control and DC offset correction.

The quadrature mixers on RX inputs 1, 3, and 5 are non-chopped “passive” mixers built with a quad ring of CMOS transmission gates. The quadrature mixers on RX inputs 2 and 4 use dynamic matching (chopping) [9] – [10] to improve second order intermodulation (IP2), flicker noise and DC offset. The chopping mixers are built with three mixers in series where each mixer is built with a quad ring of CMOS transmission gates.

Because the mixer design is “passive” (with active CMOS devices acting as switches), excellent power drain, linearity and noise figure are achieved. Current drain from the 1.2V supply of the LO buffers for the non-chopped I/Q mixers is about 3.7 mA typical, at 1 GHz while IIP3 of the mixers is around +17 dBm. Noise figure of the mixers is about 5 dB (essentially equal to the conversion loss). All of the mixer current drain comes from the LO buffers and multiplexers, since there is no DC current drain in the actual mixer switching CMOS devices. The drain with the chopping mixers is somewhat higher than the non-chopped mixers due to the additional chopping clock buffers, and depends on the value of the chopping frequency.

The filter architecture has four poles of filtering with two real poles and one complex pole pair in the Sallen-Key BiQuad. Filter bandwidth is programmable from 4 KHz to 10 MHz in 6.25% steps or less. Sufficient margin is built into the design to allow for a 20% change in RC tolerance and maintain the bandwidth range of 4 KHz to 10 MHz. Bandwidth selection is implemented by adjusting the resistor and capacitor values in the filter design. The user has independent control of the pole locations of the post mixer amplifier (PMA), voltage gain amplifier (VGA) and BiQuad as well as control of the BiQuad filter Q. This allows the user to have the flexibility to trade off filter shape and attenuation for pass-band amplitude and phase distortion to suit his application.

Baseband filter gain control is accomplished at three points. A programmable resistor divider at the input of the PMA allows attenuation in four 6 dB steps while maintaining an input impedance of 2 KΩ differential. The PMA has a maximum gain of 32 dB and a minimum gain of -10 dB. The VGA has a gain range of 8 dB and the output buffer has a programmable gain control of 0 to 18 dB in 6 dB steps. The entire baseband filter lineup has a maximum gain of 64 dB and a minimum gain of -4 dB.

A unique feature of the baseband filter is the use of chopper stabilization to mitigate the undesirable effects that occur in direct conversion receivers when designed in a CMOS process. Three of these drawbacks are susceptibility to flicker noise, DC offset and 2nd order intermodulation distortion.

Chopper stabilization is implemented around the first stage amplifier of each two-stage op-amp. This implementation was chosen due to the fact that the op-amp’s input referred voltage offset and flicker noise performance are heavily dependent on the first stage of the op-amp. The chopper frequency is derived from the crystal input and can be selected as a divide by 1, 2, 4 or 8 of the crystal frequency. Flicker noise is essentially eliminated when chopping is enabled and thus narrowband protocols will see improvement in receiver sensitivity. The measured performance of chopper stabilization is shown in Fig. 3.

![Fig. 3. Received signal spectrum with and without chopping.](image)

DC offset correction circuitry (DCOC) is implemented as a complete control loop that automatically corrects DC offsets at the output of the baseband filter. DCOC consists of a 1-bit ADC (comparator), control logic, and a 5-bit current mode DAC that injects current into the feedback resistors of the VGA to adjust the offset voltage. The control logic implements a successive approximation

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algorithm that converges on the correct 5-bit word that compensates for the filter’s DC offset.

B. Transmitter

The transmit direct launch quadrature modulator will support both linear and constant envelope modulation formats to cover standards with baseband bandwidths of 4 KHz to 10 MHz (channel bandwidths of 8 KHz to 20 MHz) and RF carrier frequencies from 100 MHz to 2.5 GHz. There are two fully differential modes of operation – classical I/Q or polar (with an external PA). In either case, baseband bandwidths and output power are programmable to meet the spectral mask requirements of a given protocol. For narrow and medium band protocols, a Cartesian feedback system provides the necessary linearization. This system requires a downmix path (receiver) that samples the output of the power amplifier and uses that sampled signal to correct for any non-linearity induced errors in the forward transmission path.

The baseband transmit block provides filtering, programmable attenuation, level shifting and buffering for the DAC inputs and drives the forward RF section and/or the Cartesian baseband forward path. The input buffers provide stepped attenuation for the incoming baseband signals. Programmable active RC reconstruction filters limit the amount of far out quantization noise and images due to aliasing. An RC tracking oscillator provides automatic filter pole adjustment for the reconstruction filters. Closed loop correction of baseband DC offsets and I/Q phase gain imbalance is done in the pre-transmit warm-up period.

The forward RF chain contains three separate RF mixer/driver paths along with the associated biasing and gain control. Each path is independently programmable to trade off bandwidth, power control range, and linearity according to the signal protocol being processed.

The Cartesian feedback path is essentially a highly linear direct conversion receiver with low sensitivity. The output of the external power amplifier is coupled into the RF inputs of this block where the signal is either amplifier or attenuated and then down converted to baseband using the down-mixer and feedback LO. Two baseband amplifiers provide programmable gain for the feedback signal before being fed into the Cartesian forward path. With its programmable gain control, this block provides the feedback gain in the Cartesian system that ultimately controls the output power of the transmitter. Two 6-bit DC offset DACs tune out any offset errors at 2.5 mV per step.

C. Frequency Synthesizer

Direct digital synthesis is used to supply LO signals for the receiver and transmitter (forward and reverse paths) as well as the clock for the chopping mixers. DDS has a feature set that makes it attractive in SDR applications. A very wide tuning range can be achieved with a single VCO. In our chip, a single VCO provides the 1 GHz clock to the digital processing blocks of multiple independent DDSs, each of which can be tuned independently and with phase coherent properties. This arrangement is immune to VCO pulling (or transmit re-modulation) [11] since the VCO is not operating at the DDS output frequency. Each DDS generates square wave outputs with fast rise and fall times that are ideal to drive the switching mixers in the receiver and transmitter. Finally, the cycle-to-cycle frequency switching enables unique transceiver capabilities that are not possible with traditional phase locked loops with their associated lock times.

Traditional direct digital synthesizers have two disadvantages relative to PLL-based synthesizers – power consumption and spurious frequency content. The DDS architecture developed in Motorola Labs [12]-[14] uses a ROM-less architecture to achieve typical power consumption below 120 mW and non-zero-mean dither [15] to keep spurious frequency components below -35 dBc.

The differential I and Q outputs can switch frequency on a (glitch free) cycle-to-cycle basis anywhere from 100 MHz to 2.5 GHz. With 15 Hz resolution and measured phase noise of -123 dBc/Hz at 25 KHz offset and -150 dBc/Hz at 20 MHz offset, the DDS has the flexibility and the noise and switching time performance that is needed for SDR applications.

III. MEASURED RESULTS

The chip was fabricated in a 6-metal 90 nm CMOS process. A photograph of the 4 by 5 mm die is shown in Fig. 4.
The divergent requirements of the many standards this RFIC can process, makes a comprehensive performance report beyond the scope of this paper. While certain parameters may be optimized based on a particular standard, measured data based on typical conditions are listed in Table I.

**Table I**

<table>
<thead>
<tr>
<th>Summary of Transceiver Performance</th>
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<tr>
<td><strong>Freq. Range</strong></td>
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<tr>
<td>Rx NF</td>
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<tr>
<td>Rx Gain</td>
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<tr>
<td>Rx IIP2</td>
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<tr>
<td>Rx IIP3</td>
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<tr>
<td>Rx Current Drain</td>
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<tr>
<td>Tx Output Power</td>
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<tr>
<td>Tx Sideband Suppression</td>
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<tr>
<td>Tx Current Drain</td>
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<tr>
<td>EVM π/4 DPQSK 3.5 MS/s</td>
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<tr>
<td>LO Phase Noise</td>
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<tr>
<td>LO Frequency Resolution</td>
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<td>LO Current Drain per DDS</td>
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**IV. CONCLUSION**

An all CMOS transceiver suitable for portable equipment SDR and Cognitive Radio applications has been implemented in 90 nm technology. The transceiver provides continuous receiver and transmitter coverage from 100 MHz to 2.5 GHz. It utilizes programmable low pass filters with bandwidth selectable in 10% steps from 4 KHz to 10 MHz. Technical issues associated with direct conversion receiver technology were overcome with a novel implementation of dynamic matching. A universal transmitter was implemented with direct launch quadrature modulation using a DDS solution that overcomes frequency pulling also known as transmitter re-modulation. A universal transmitter was implemented with direct launch quadrature modulation using a DDS solution that overcomes frequency pulling also known as transmitter re-modulation. Differential transmitter output power of +6 dBm with 80 dB of 1 dB resolution power control was implemented with a power dissipation of 180 mW. A Cartesian feedback network is included to provide up to 30dB of adjacent channel coupled power transmitter linearization improvement at 25 KHz offset, maintained over a 30 dB power control range. Only a single reference voltage controlled oscillator (VCO), operating at a single frequency is required by using DDS signal source technology instead of phase lock loop signal synthesis.

A flexible, yet economical with low power dissipation, reconfigurable transceiver platform suitable for all present and future wireless transceiver applications is the objective. This transceiver design is a significant step in achieving this goal and provides a platform for SDR/ Cognitive radio test and evaluation. Future areas of SDR efforts are focused on including reconfigurable data converters, universal baseband communication processor, universal RF power amplifier, programmable receiver & transmitter selectivity, and software articulated antennas.

**REFERENCES**